Thin Solid Films 542 (2013) 242–245

Contents lists available at SciVerse ScienceDirect

Thin Solid Films

journal homepage: www.elsevier.com/locate/tsf

Improvement of charge trapping characteristics of Al_2O_3/Al-rich Al_2O_3/SiO_2 stacked films by thermal annealing

Shunji Nakata [a],*, Takashi Kato [b], Shinya Ozaki [b], Takeshi Kawae [b], Akiharu Morimoto [b]

[a] NTT Microsystem Integration Laboratories, Atsugi 243-0198, Japan
[b] Graduate School of Natural Science and Technology, Kanazawa University, Kanazawa 920-1192, Japan

ARTICLE INFO

Article history:
Received 14 May 2012
Received in revised form 29 May 2013
Accepted 6 June 2013
Available online 18 June 2013

Keywords:
Radio-frequency magnetron sputtering
Oxides
Aluminum oxide
Silicon dioxide
Charge trapping
Capacitance–voltage measurements
Thermal annealing

ABSTRACT

Thin film Al_2O_3/Al-rich Al_2O_3/SiO_2 structures were fabricated on p-Si substrates. Radio-frequency magnetron co-sputtering was used to form Al-rich Al_2O_3 thin film as the charge-trapping layer of nonvolatile Al_2O_3 memory. Capacitance–voltage measurements showed a large hysteresis due to charge trapping in the Al-rich Al_2O_3 layer. The charge trap density was estimated to be 42.7×10^{18} cm^{-3}, which is the largest value ever reported for an Al-rich Al_2O_3 layer; it is six times larger than that of a conventional metal–nitride–oxide–silicon memory. Thermal annealing was found to reduce the leakage current of the Al_2O_3 blocking layer, thereby providing this structure with better data retention at room temperature than an as-deposited one. In addition, the annealed structure was found to exhibit good data retention even at 100 °C.

1. Introduction

Nonvolatile semiconductor memory devices are being widely studied because of their low-power operation, high memory density per volume, and other attractive features. Charge trap memories [1–7] are a subject of special interest for nanoscale devices [8–11] because their simple structure should enable extremely large-scale integration.

Recently, we fabricated a simple trap memory consisting of a SiO_2 tunneling insulator, an Al-rich Al_2O_3 charge trapping layer, and an Al_2O_3 blocking insulator [12]. The capacitance–voltage (C–V) characteristics exhibit a large hysteresis. This is a promising structure because the layer on the tunneling insulator contains only two elements (Al, O). Although this simple gate structure is suitable for a low-cost memory, there are a couple of problems with it. One is that there are large defects in the Al_2O_3 blocking layer because the sample was not annealed after deposition. Another problem is that the use of a low-resistivity wafer ($\rho \cong 1.5 \times 10^{-2}$ Ω cm) makes the width of the semiconductor depletion layer, W, small. This makes the capacitance, C_D, of the semiconductor depletion layer large, which results in a large minimum capacitance, C_{min}, in the C–V curve, where C_{min} equals the series capacitance of C_D and the gate insulator capacitance, C_i. In consequence, there is a small difference between the capacitance after writing and that after erasing, which is not suitable for capacitance measurements. One more problem is that the sample was made on an n-Si wafer, for which the carriers are holes and the mobility is low.

In this study, we fabricated an Al_2O_3/Al-rich Al_2O_3/SiO_2 structure on a p-Si substrate with a high resistivity ($\rho \cong 1$ Ω cm) to obtain a smaller C_{min} and thus a larger difference between the capacitance after writing and that after erasing. Moreover, the use of a p-Si substrate, for which the carriers are electrons, also provides a higher mobility. We used this structure to investigate the effects of annealing by comparing the C–V characteristics of as-deposited and annealed samples. We also investigated data retention by measuring the timewise change in capacitance at room temperature and at 100 °C.

2. Experiments

2.1. Film deposition

Radio-frequency (RF) magnetron co-sputtering was used to form Al-rich Al_2O_3 [13]. Al metal plates were placed on an Al_2O_3 target, and the Al content of the Al–O film was controlled by means of the areal ratio of the Al on the target.

Sputtering was carried out with Ar gas at a flow rate of 2 sccm, a pressure of 0.267 Pa, an RF power of 100 W, and an RF frequency of 13.56 MHz. The thickness of deposited film was measured with a spectroscopic ellipsometer. The Al content of the Al–O film was investigated with an electron probe micro-analyzer.

---

* Corresponding author. Faculty of Engineering, Kinki University, Higashi-hiroshima 739-2116, Japan. Tel.: +81 462402858.
E-mail addresses: nakata@hiro.kindai.ac.jp (S. Nakata), amorimot@ec.t.kanazawa-u.ac.jp (A. Morimoto).

0040-6090/$ – see front matter © 2013 Elsevier B.V. All rights reserved.
http://dx.doi.org/10.1016/j.tsf.2013.06.005

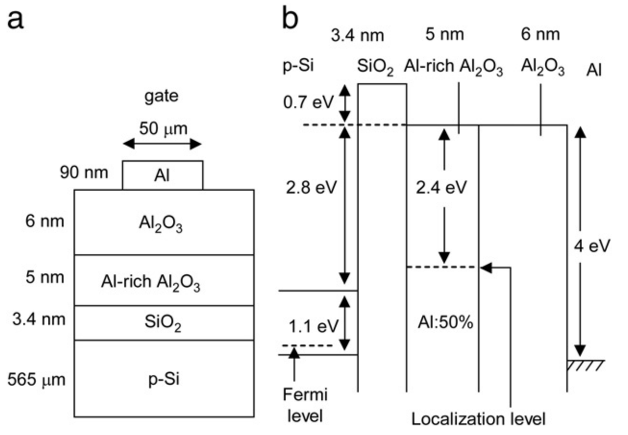

Fig. 1. Structure of sample with Al-rich Al_2O_3: (a) cross section and (b) energy band diagram.

The samples were made on (100) p-Si substrates. First [Fig. 1(a)], the wafers were cleaned with HF for 40 s, and thermal oxidation formed a layer of SiO_2 as a tunnel barrier insulator. The oxidation was carried out in a gas mixture (N_2:O_2 = 3:1) at a temperature of 1000 °C for a period of 180 s. It resulted in a 3.4-nm-thick layer of SiO_2.

Next, a 5-nm-thick layer of Al-rich Al_2O_3 as a charge storage layer was deposited by co-sputtering. The Al content was as high as 50%, which is larger than the 40% for stoichiometric Al_2O_3. Then, RF sputtering deposited a 6-nm-thick layer of stoichiometric Al_2O_3 as a blocking barrier insulator. After deposition, the samples were annealed in N_2 gas. The annealing process employed a linear temperature ramp to 400 °C in 1 h, followed by a 10-m hold, and a linear cool-down for 3 h. Finally, a square gate electrode with a width of 50 μm was formed by the thermal evaporation of Al at a pressure of 1.33×10^{-4} Pa. In the band diagram of this structure [Fig. 1(b)], the height of the Al_2O_3 conduction barrier is 2.8 eV with respect to the Si conduction band [14,15] and 4 eV with respect to the Al Fermi level [16]. In contrast, the height of an HfO_2 conduction barrier is only 1.5 eV with respect to the Si conduction band [15]. So, the barrier height is larger for Al_2O_3/Si than for HfO_2/Si. This high barrier is better at trapping carriers, which makes it more suitable for making nonvolatile memory. The role of the localized energy level due to Al-rich AlO is to trap a carrier in the level or release it from the level.

2.2. Capacitance–voltage characteristics

We measured the high-frequency C–V characteristics of as-deposited and annealed Al-rich Al_2O_3 structures with an Al content of 50%. The measurements were performed at a frequency of 1 MHz at room temperature. The p-Si wafer was connected to the ground. The maximum applied gate voltage was 4, 5, 6, or 7 V. When the maximum applied gate voltage was 4 V, the voltage to the gate electrode was swept from 4 V down to −4 V and then back up. The sweep rate was about 1 V/s. The C–V curves for as-deposited [Fig. 2(a)] and annealed [Fig. 2(b)] samples show a large hysteresis due to charge trapping in the Al-rich Al_2O_3 layer. The large hysteresis for the annealed sample shows that the Al-rich Al_2O_3 structure is stable after annealing at a high temperature, such as 400 °C. Moreover, the hysteresis curve for the annealed sample does not show any deviations from the ideal one and is almost the same as the ideal one, while that for the as-deposited sample shows deviations. This strongly suggests that annealing reduces the number of defects in the Al_2O_3 blocking layer. The types of defects that cause the deviation are not well understood yet, and further research is necessary to clarify their origin.

Next, we examined whether or not the measured capacitance agreed with the theoretical one calculated from metal–insulator–semiconductor theory. This is very important for determining the electrical field across each layer. The insulator capacitance, C_i, was estimated to be about 10 pF from Fig. 2(a) and (b). It is equal to the series capacitances of the SiO_2, Al-rich Al_2O_3, and Al_2O_3; thus, $1/C_i = 1/C_{SiO_2} + 1/C_{Al-O} + 1/C_{Al_2O_3}$. From the dielectric constant of SiO_2 (3.9), we estimated C_{SiO_2} to be $3.9 \times \varepsilon_0 S/3.4$ nm, where ε_0 is the vacuum permittivity and S is the sample area. Assuming that $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m and $S = 2500\ \mu m^2$ yields $C_{SiO_2} = 25.4$ pF. Now, the dielectric constant of Al-rich Al_2O_3 with an Al content of 50% is 8.2, which is almost the same as the value of 8.1 for Al_2O_3 [12]. So, to simplify the calculations, we set the dielectric constant of both materials to 8. Recent experimental results have confirmed this value [17]. Using this dielectric constant, C_{Al-O} and $C_{Al_2O_3}$ were estimated to be 35.4 and 29.5 pF, respectively. These values yield an insulator capacitance, C_i, of 9.9 pF, which agrees well with the measured value of 10 pF.

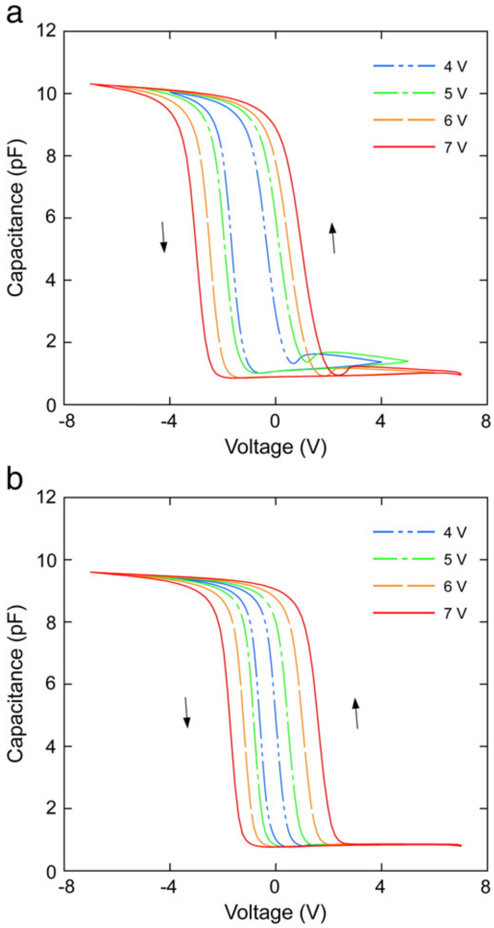

Fig. 2. C–V characteristics of Al-rich Al_2O_3 layer: (a) as-deposited and (b) annealed.

Next, let us consider C_{min}, which is the value when V = 7 V in Fig. 2. As previously mentioned, C_{min} is the series capacitance of C_i and the capacitance of the semiconductor depletion layer, C_D: $1/C_{min} = 1/C_i + 1/C_D$. C_D is given by $C_D = \varepsilon_{Si} S/W$, where ε_{Si} is the permittivity of Si, and W is the width of the semiconductor depletion layer. The formula for W is [18]

$$W^2 = \frac{4\varepsilon_{Si} kT}{q^2 N_A} \ln\left(\frac{N_A}{n_i}\right) , \qquad (1)$$

where k is the Boltzmann constant, q is the elementary charge, N_A is the impurity concentration, and n_i is the intrinsic carrier density. From the resistivity of the p-Si wafer, we estimated N_A to be $1.3 \times 10^{16}\ cm^{-3}$ [18]. Thus, assuming that $n_i = 1.45 \times 10^{10}\ cm^{-3}$ yields $\ln(N_A/n_i) = 13.7$. If we further assume that $T = 293$ K and $\varepsilon_{Si} = 11.9 \times 8.85 \times 10^{-12} F/m$, the width, W, is 265 nm. Thus, $C_D = \varepsilon_{Si} S/W = 1.0$ pF. Using the values