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Critical review

Growth, dielectric properties, and memory device applications of ZrO_2 thin films

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A R T I C L E I N F O

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A B S T R A C T

In the advancement of complementary metal-oxide-semiconductor device technology, SiO_2 was used as an outstanding dielectric and has dominated the microelectronics industry for the last few decades. However, with the recent size downscaling, ultrathin SiO_2 is no longer suitable. ZrO_2 has been introduced as a high-*k* dielectric to replace SiO_2. This paper reviews recent progress of ZrO_2 thin films as dielectric layers for volatile dynamic random access memory (DRAM) applications and as a gate dielectric for CMOS devices. Materials and electrical properties of ZrO_2 films obtained by different deposition methods are compared. The effects of different top and bottom electrodes, and different doping elements, on ZrO_2 dielectric properties are described. Applications discussed include the use of ZrO_2 in Ge and SiGe nanocrystal-embedded nonvolatile flash memory devices. ZrO_2 films as charge trapping layers in SOZOS (poly-Si/SiO_2/ZrO_2/SiO_2/Si) and TAZOS (TaN/Al_2O_3/ZrO_2/SiO_2/Si) based nonvolatile flash memory stacks, and bipolar, unipolar, and nonpolar ZrO_2-based resistive switching memory devices are also briefly discussed. The impact of electrode materials, metal nanocrystals, metal implantation, metal doping, metal layers, and oxide ion conductor buffer layer on resistive switching properties and switching parameters of emerging ZrO_2-based resistive switching memory devices for high speed, low power, nanoscale, nonvolatile memory devices are briefly reviewed. A roadmap of the applications of ZrO_2 thin film in future low power, nanoscale microelectronic device applications is realized from this review.

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1. Introduction

The rapid progress of complementary metal-oxide-semiconductor (CMOS) integrated circuit (IC) technology, since the late 1980s, has enabled the silicon-based microelectronics industry to concurrently meet several technological requirements to fuel market expansion. These requirements include high performance (speed), high reliability, high package density, increased low voltage and low power applications, and multilevel capability (MLC) [1]. The incredible characteristic of transistors that drives the rapid growth of the semiconductor industry is that their speed increases and their cost decreases as their size is reduced. To meet these requirements for future CMOS technology nodes, device scaling has acted as the driving force. CMOS transistor scaling has been the primary factor driving improvements in microprocessor performance. Recently, however interest in nonvolatile memory technology research is increasing rapidly due to a vast number of applications in portable electronic devices which play an important part in our daily life [2,3]. Memory devices are classified into two broad categories based on CMOS technology: volatile and nonvolatile. Fig. 1 is a flow chart classifying semiconductor memory devices [2].

Downsizing of MOSFETs (metal-oxide semiconductor field effect transistors) places stringent demands on the properties of the gate oxide. SiO_2 has dominated the silicon microelectronics industry as the most practical choice for an FET (field effect transistor) gate dielectric material since 1957. SiO_2 offers several crucial advantages such as being highly compatible with silicon technology, a uniform and conformal oxide, high interface quality etc. Industry's acquired information regarding SiO_2 properties and processing techniques over the past several decades makes change difficult. However, further scaling of the FET is eventually going to be impeded by the inability to reduce the oxide thickness below 1.3 nm. For thin SiO_2, the leakage currents from electron tunneling through the dielectrics are a problem.

Amorphous HfO_2 and ZrO_2 with dielectric constants (k) ~20, have been considered for several years as SiO_2 replacement candidates essentially due to their good physical and electrical properties and the fact that they can survive transistor processing [4,5]. For future technology nodes, aggressive scaling to less than 1 nm equivalent oxide thickness (EOT) will require new gate oxides with k values of more than 30 [4]. High-k oxides ($k > 50$) are also required for next generation dynamic random access memories (DRAM), where extremely low EOT (0.5 nm) is essential. Indeed, HfO_2 dielectrics are already in production for 45-nm CMOS technology by major IC manufacturers. Some leading companies are also using ZrO_2 as a dielectric material for CMOS applications. One of the most promising candidates for SiO_2 replacement, which is thermodynamically stable with respect to solid state reaction with silicon, is ZrO_2 [6–8]. In addition, it has a large band gap (~5.8 eV) and high dielectric constant (20) [9–14]. As a thin film, ZrO_2 normally condenses on a substrate in crystalline form, but amorphous ZrO_2 thin films are preferred for microelectronic device applications. Grain boundaries in crystalline ZrO_2 thin films can cause undesired increase in leakage current characteristics. Different anisotropic crystalline phases, such as monoclinic, tetragonal, and cubic [12–14], can lead to non-uniformities in k value as a function of film thickness.

A high k value is the first requirement in selecting a material for gate oxide applications. It must be higher than the k (3.9) value of SiO_2, preferably in the range 10–30 [12–30]. Several binary oxides such as Ta_2O_5, Y_2O_3, Al_2O_3, HfO_2, ZrO_2, and TiO_2 [12–30] and also perovskite materials such as $SrTiO_3$ and $(Ba,Sr)TiO_3$ [21–23], have been investigated as oxide dielectric materials for CMOS devices. If the k value of the material is too high, such as for TiO_2 (k~80), fringing

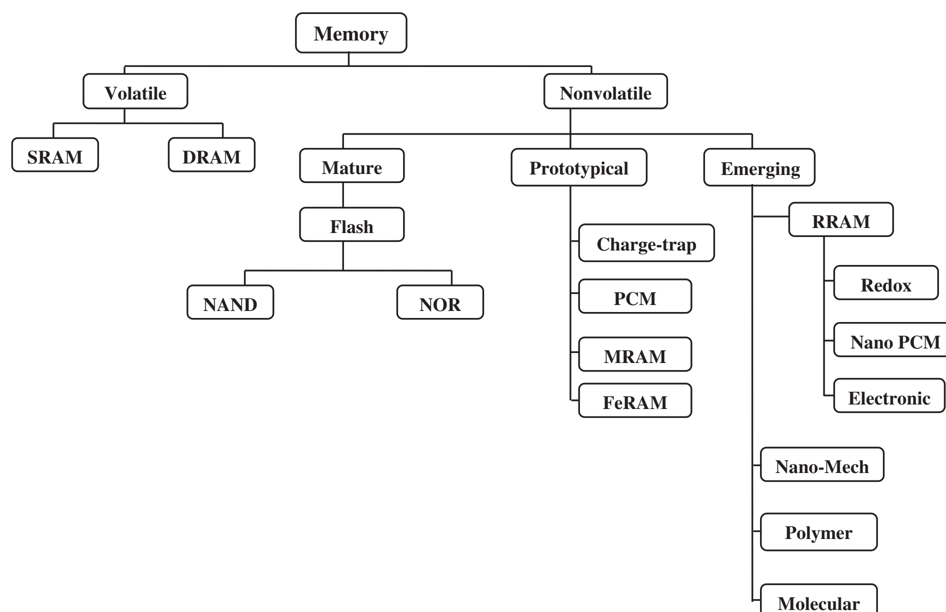

Fig. 1. Classifications of semiconductor memory [2]. SRAM: Static random access memory, DRAM: Dynamic random access memory, PCM: Phase change memory, MRAM: Magnetic random access memory, FeRAM: Ferroelectric random access memory, and RRAM: Resistive random access memory.

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