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Thermal oxidation and encapsulation of silicon–carbon nanolayers

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ABSTRACT

Silicon–carbon (Si–C) thin films play a key role in many technological applications such as hard coatings, high-power electronics, and photovoltaics. In photovoltaics in particular annealed Si–C thin films containing Si quantum dots are used to develop solar cells with improved efficiency. The oxidation of these films during the annealing step, which is unavoidable in the high-throughput processes required for photovoltaics, was explored using scanning electron microscopy, Fourier-transformed infrared spectroscopy, and X-ray photoelectron spectroscopy. SiO_2 surface layers 5 to 14 nm thick were observed even in nominally inert furnace atmospheres, while annealing with graphitic carriers leads to the formation of SiO_xC_y films a few nm thick. To avoid the formation of either compound and thereby reduce the impact of the particular furnace used on the Si–C film an encapsulation layer made of a-Si:H was developed. It is shown that 40 nm of this layer can protect an Si–C film from oxidation. The SiO_2 and residual Si formed are removed using standard etchants with only minimal impact on the Si–C film. It was found that this process depends critically on the thickness of a-Si:H deposited but is fairly insensitive to the parameters of the etching process. The encapsulation process presented herein is a key step towards the fast large-scale annealing of Si–C films required for photovoltaic applications, and has the potential to greatly simplify the thermal treatment of a wide range of thin films.
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1. Introduction

Silicon–carbon (Si–C) thin films play a key role in a wide variety of technologically important applications, ranging from hard coatings for drills to single crystal semiconductor layers for high-power and high-temperature electronics applications [1–3]. They are also gaining significance in photovoltaics, where hydrogenated amorphous silicon carbide films (a-Si_xC_{1-x}:H) find usage as passivation layers [4], window layers [5], and heteroemitters [5], while polycrystalline SiC is used for diffusion barriers [6,7] for thin-film cells on low-cost substrates. Most recently, SiC has been investigated as a potential host matrix for silicon quantum dots [8–10] which can be produced by annealing a stack of alternating ultrathin layers of stoichiometric (a-SiC:H) and silicon-rich (a-Si_xC_{1-x}:H, $x>0.5$) silicon carbide at high temperature to form quantum-dot sized silicon precipitates in SiC. Si quantum dots have a larger band gap than bulk Si [11], which means that a solar cell with an Si quantum dot absorber could be combined with a regular Si cell to create a tandem cell that circumvents the single-cell efficiency limits that restricts the performance of standard Si solar cells [12] while remaining compatible with standard Si solar cell processing, permitting a rapid process transfer to industry. SiC is an ideal host matrix for Si quantum dots, as the small conduction and valence band offsets [8] offer a good compromise between the quantum confinement in Si and carrier mobility [13].

To form the quantum dots, a precise control of layer thicknesses during deposition as well as a high temperature annealing step is required. However it is well-known that SiC, much like Si, forms a native oxide under standard conditions and oxidises further upon annealing in an oxygen-containing atmosphere [14–19]. This is undesirable if an electrical contact must be made to the SiC surface. Most of the literature [14,16–18] reports the oxidation of SiC to form SiO_2, which is readily removed with HF; SiC acts as an etch stop for this chemical. However, this is not a viable process for stacks of ultrathin layers as control over the number of layers and over the nature of the surface layer is lost if oxidation is non-uniform. Furthermore, some authors [15,19,20] report the formation of a ternary SiO_xC_y compound which is not readily removed by HF [19]. It is therefore of fundamental importance to protect these stacks of ultrathin layers from oxidation, a viable method being the deposition of another film on top of the a-Si_xC_{1-x}:H/a-SiC:H multilayer which stops oxidation during annealing and can be readily removed afterwards. This processing route would lead to a precise control of the annealed multilayer irrespective of any reactions that occur between the sample surface and the furnace atmosphere, making it the perfect solution for high-throughput production which is indispensable for cost-effective photovoltaics.

In this paper, we begin by presenting results on the oxidation of a-Si_xC_{1-x}:H/a-SiC:H multilayers during annealing to show that complete suppression of oxidation is extremely difficult, and then present

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a capping layer made of hydrogenated amorphous silicon (a-Si:H) which prevents oxidation and is readily removed by wet chemistry.

2. Experimental details

The a-Si_xC_{1-x}:H films were deposited on 10 Ω cm p-type float-zone (FZ) silicon wafers. The wafers were cleaned in HNO_3 and HF before film deposition. The films were deposited by plasma-enhanced chemical vapour deposition (PECVD) using a Roth&Rau AK400 reaction chamber and precursor gases silane (SiH_4), methane (CH_4), hydrogen (H_2) and argon (Ar) for the different films. Gas flows for the different layers are shown in Table 1. The process parameters were 65 W high frequency (13.56 MHz) with a plasma power density of 100 mW cm^{-2}, 30 Pa pressure and a substrate temperature of 270 °C. Immediately prior to deposition, the substrates were exposed to hydrogen gas (100 sccm H_2) for 5 min to remove contaminants and the native oxide.

Three sets of samples were deposited: one set of single a-SiC:H layers 300 nm thick, one set of multilayers consisting of 15 nm a-SiC:H and 20 bilayers of 4 nm a-Si_xC_{1-x}:H/4 nm a-SiC:H, and one set identical to the latter, but capped with 40 nm a-Si:H. The multilayer samples with and without a-Si:H capping layers have very similar structures to the multilayers used to produce Si nanocrystals in SiC [19,21,22], such that the results presented herein are directly relevant to this research. The single a-SiC:H layers are deposited specifically for X-ray photoelectron spectroscopy (XPS) because having a layer of known composition permits a more in-depth analysis of the data.

Samples from each set were then annealed at 1050 °C for 60 min in three different furnaces, here referred to as furnaces A, B and C. Key furnace parameters are shown in Table 2. Furnace B is a conventional resistance-heated horizontal tube furnace from Centrotherm designed for 4 in wafers. Furnace A is similar to furnace B but only 2 in in diameter, and is additionally evacuated to 3×10^{-4} Pa at 150 °C to remove residual oxygen from the furnace and surface contaminants from the samples before flooding with nitrogen and heating to 1050 °C. Furnace C is an optically heated furnace where annealing is done in an Ar atmosphere.

After annealing, films capped with a-Si:H had the surface oxide removed with a 60 s etch in 1% HF and residual silicon with a 20 s etch in CP_{33} or KOH solutions. CP_{33} is a mixture of HF, HNO_3 and CH_3COOH in the proportions 1:6:2, is used at room temperature and has an etch rate of approximately 5 μm/min for Si. KOH is used at a concentration of 20% at 80 °C and has an etch rate of approximately 1 μm/min.

A Woollam M-2000 spectroscopic ellipsometer was used for determination of as-deposited film thicknesses, while thicknesses of annealed films were determined using a Hitachi SU70 scanning electron microscope (SEM) equipped with a cold trap and operated at 5 kV. Fourier-transformed infrared (FTIR) spectroscopy was carried out using a Bruker IFS 113v in the range of 400 cm^{-1} to 4000 cm^{-1} with 6 cm^{-1} resolution. Samples for infrared spectroscopy had the rear side oxide selectively removed by inkjet printing a hotmelt resist onto the front side, followed by a 60 s etch in buffered HF and stripping of the resist in acetone. XPS was done using a Physical Electronics 5600 operated with an MgKα source. The electrons were detected at a take-off angle of 45° using a pass energy of 23.5 eV. Atomic force microscopy (AFM) was done using a Veeco D3100 operated in intermittent contact (tapping) mode and equipped with a TAP 300 G Si tip from Budget Sensors with a tip radius of ca. 10 nm. Images of a 1 μm^2 area were acquired at 1 μm/s at a resolution of 1024 × 1024.

Table 1
Gas flows used for PECVD of the different layers, in sccm.

	SiH_4	CH_4	H_2	Ar
a-Si_xC_{1-x}:H	10	10	100	0
a-SiC:H	7	60	100	0
a-Si:H	30	0	100	30

Table 2
Furnaces used for annealing.

Furnace	Atmosphere	Entry temperature	Heating rate	Carrier
A	N_2 (purified)	25 °C	10 °C/min	Quartz
B	N_2	850 °C	10 °C/min	Quartz
C	Ar	25 °C	300 °C/min	Graphite

3. Results and discussion

The a-Si_xC_{1-x}:H/a-SiC:H multilayer films were annealed in the three furnaces described above. Once annealed, the films contain both amorphous and nanocrystalline Si and SiC, and will be referred to as Si–C films for simplicity, together with the letter of the furnace they were annealed in. All furnace annealing was carried out in inert atmospheres, which means no oxide should form on the samples during annealing. Nevertheless, an SEM cross-section of sample B shows a 14 nm ± 5 nm thick surface layer resembling a surface oxide on top of the 130 nm thick Si–C film (Fig. 1). SEM images of sample A exhibited an 11 nm ± 5 nm thick surface layer. It is worth pointing out that the thicknesses of these films cannot be determined using ellipsometry because no accurate optical model exists for the annealed Si–C film.

FTIR spectroscopy was used to check whether these surface films really are surface oxides. The spectra, shown in Fig. 2, were measured on samples on Si substrates that had had the SiO_2 on the rear side removed, i.e. any Si–O–Si peaks at 1080 cm^{-1} [23] stem from the oxide formed on the Si–C film only. The spectra of samples A and B clearly show Si–O–Si peaks, and the film annealed in furnace B shows both the larger Si–O–Si FTIR peak and the thicker surface film in SEM. This confirms that the surface layers observed in the SEM are indeed surface oxides brought about by the reaction of the films with residual oxygen in the furnaces. Using the oxide thickness and total sample thickness measured on the SEM images, we deduce that 1 to 2 of the 20 bilayers deposited were oxidised.

This significant oxidation is surprising; particularly furnace A, which is evacuated at room temperature and flooded with purified N_2 before annealing begins, would not have been expected to cause oxidation. It is only sample C which does not exhibit an Si–O–Si peak — it actually has a dip at the Si–O–Si peak position which will be discussed later. We attribute the apparent absence of a thermal oxide on sample C to the graphitic sample carriers in the furnace with which the oxygen reacts preferentially. However, graphitic carriers are not ideal for Si–C films because they can influence the film stoichiometry and contaminate the sample, limiting further processing and electrical and photovoltaic performance. The absence of a Si–O–Si peak in the spectrum

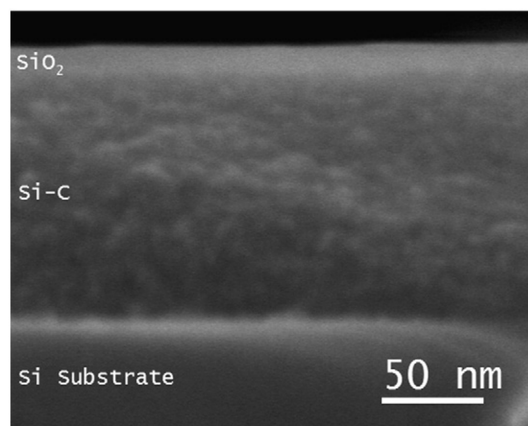

Fig. 1. Scanning electron micrograph of an Si–C film annealed in furnace B.

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