



Analysis of Total Ionizing Dose effects for highly scaled CMOS devices in Low Earth Orbit

Muhammad Sajid^{a,*}, N.G. Chechenin^b, Frank Sill Torres^c, Muhammad Nabeel Hanif^d,
Usman Ali Gulzari^e, Shakaib Arslan^f, Ehsan Ullah Khan^g

^a Department of Electrical Engineering, CIIT, Islamabad, Pakistan

^b Skobel'syn Institute of Nuclear Physics, Moscow State University, Russia

^c Cyber-Physical Systems, DFKI GmbH, Bremen, Germany

^d Satellite Research & Development Center, Lahore, Pakistan

^e Department of Electrical Engineering, University of Lahore, Islamabad, Pakistan

^f Department of Physics, Riffah International University, Islamabad, Pakistan

^g Department of Physics, International Islamic University, Islamabad, Pakistan

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ABSTRACT

Total Ionizing Dose (TID) effects are an essential concern for integrated devices that are operating in space environment. We present in this work an extensive study of TID effects in Deep-Submicron and Nanoscale CMOS technologies. Principal aspects are the changes of the transistors I-V characteristics due to TID effects, the variation of the threshold voltage and the impact of radiation on the carrier densities and mobility as well as on the electrical potentials and the leakage currents. Further, we discuss a potential solution that reduces TID effects in CMOS devices. The device level simulations consider a satellite application that orbits in Low Earth Orbit (LEO), leading to dose levels of up to 500 krad(Si). Results clearly indicate the high impact of TID on the transistor parameters, enforcing the designer to consider countermeasures in order to guarantee the circuits reliability.

1. Introduction

The constant scaling of current CMOS technology impacts considerably the susceptibility of integrated circuits to Total Ionizing Dose (TID) effects [1]. This is even more critical for application in space environment with very high radiation. The main consequences of TID in CMOS devices are the accumulation of positive charges N_{ot} in the Silicon dioxide (SiO_2) layers as well as the creation of trapped interface states N_{it} between the Silicon (Si) and the oxide layers [2]. These effects can change the transistors threshold voltage V_{th} and, thus, impact the circuit performance and the leakage power consumption. Especially the latter is critical for the power budget of onboard devices in satellites [3].

We present in this work an extensive study of TID effects in CMOS devices fabricated in a Deep-Submicron (130 nm) and a Nanoscale (65 nm) technology. The devices have been simulated for conditions in the Low Earth Orbit (LEO) space environment, which is a common location for satellite applications. That means, we explored the impact of radiation dose levels from 100 krad(Si) to 500 krad(Si) with a dose rate of 10 rad/s considering a mission duration of three years. Our research

focused on charge trapping, creation of trap states and the effects on charge carrier mobility, threshold voltage shift and leakage power consumption. Further, we explored the effectiveness of Aluminum shielding in order to reduce the deposited radiation. Based on the obtained results, we propose an appropriate shield thicknesses that can guarantee a reliable operation of integrated circuits fabricated in both technologies.

The remainder of this paper is organized as follows. The following Section 2 gives preliminary information regarding TID effects in CMOS device and TID deposition in LEO. Section 3 introduces the applied analysis environment that had been applied throughout the work. Section 4 presents and discusses the obtained simulation results, while Section 5 relates to the analysis of possible radiation protection via Aluminum shielding. Finally, Section 6 concludes this work.

2. Preliminaries

This section presents basic information regarding radiation effects in integrated devices and dose deposition in LEO in order to keep this work as self-explanatory as possible.

* Corresponding author.

E-mail address: sajiddikhan@gmail.com (M. Sajid).

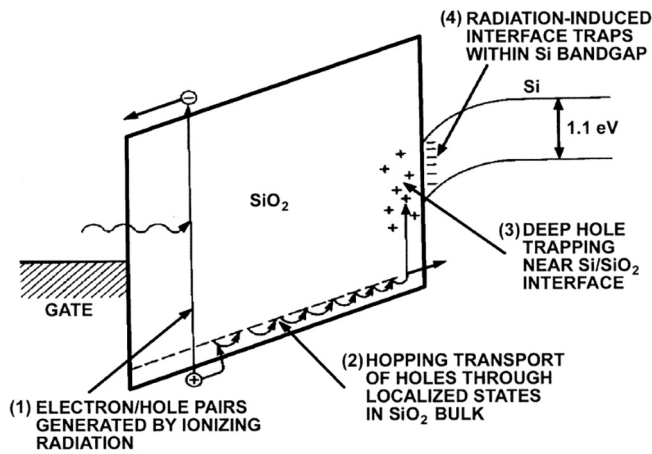


Fig. 1. Energy Band Diagram for MOS structure under TID [6].

creation of electron-hole pairs in the conduction and valence bands of the thin SiO₂ is attributed to the passage of ionized particles through the gate oxide (see (1) in Fig. 1). In the gate oxide, the electrons are considerably more mobile than holes [5]. Consequently, the electrons are swept out of the oxide very rapidly. Next, the recombination of only some fraction of these electrons and holes occurs. The remaining holes that are not recombined are relatively immobile and remain close to the location at which it has been generated. These holes are called fixed oxide charges and cause a negative shift of the threshold voltage V_{th} of the MOS device.

The second process is the transportation of holes towards the interface between the Si substrate and the gate oxide (see (2) in Fig. 1). This process is very sensitive to the applied electric field, the oxide thickness and the temperature.

The third process is related to the fraction of the transported holes that, when reaching the Si interface, fall into relatively long-time deep trap state (see (3) in Fig. 1).

The fourth process is the radiation-induced buildup of interface traps at the Si/SiO₂ interface (see (4) in Fig. 1). These traps are considered as localized states in the Si band-gap with various energy levels. The occupancy of these states is determined by the applied voltage or by the Fermi level, and thus, result into a voltage-dependent V_{th} shift.

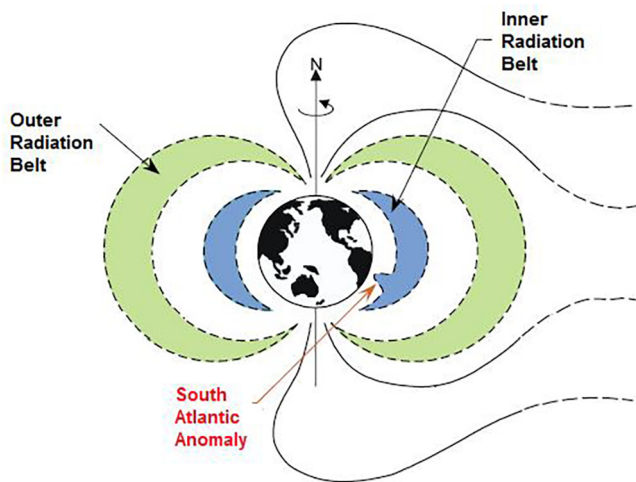


Fig. 2. Van Allen Earth Radiation Belts.

3. TID deposition at LEO altitude

In Low Earth Orbit (LEO) environment, radiation that leads to dose deposition is caused by electron and proton particles that are trapped in the Van Allen Earth Radiation Belts (ERBs) due to the earth magnetic field [7,8]. Van Allen Belts consists of inner and outer regions as well as a South Atlantic Anomaly (SAA) region, as depicted in Fig. 2. During its mission life, the orbit of a typical LEO satellite passes countless times through the ERBs. Having in mind the high radiation in these regions, it is mandatory to estimate the amount of dose deposited in the onboard electronic components in order to verify its reliability.

4. Analysis environment

In the following, we describe our analysis environment for the exploration of TID effects in integrated devices fabricated in Deep-Submicron and Nanoscale CMOS technologies and intended for satellite applications in LEO. Our analysis expects a total mission duration of three years, a typical trajectory of satellites in LEO and a device inclination of 98 degree.

Our analysis environment consists of three fundamental components: (1) a flow for the estimation of radiation a typical LEO satellite is

2.1. TID effects in MOS devices

TID effects in MOS devices comprise of four major physical processes (see also Fig. 1). The first one is the generation and recombination of electron-hole pairs. It is known that the thin SiO₂ gate insulator is considered as the most sensitive part of a MOS device to TID [4]. The

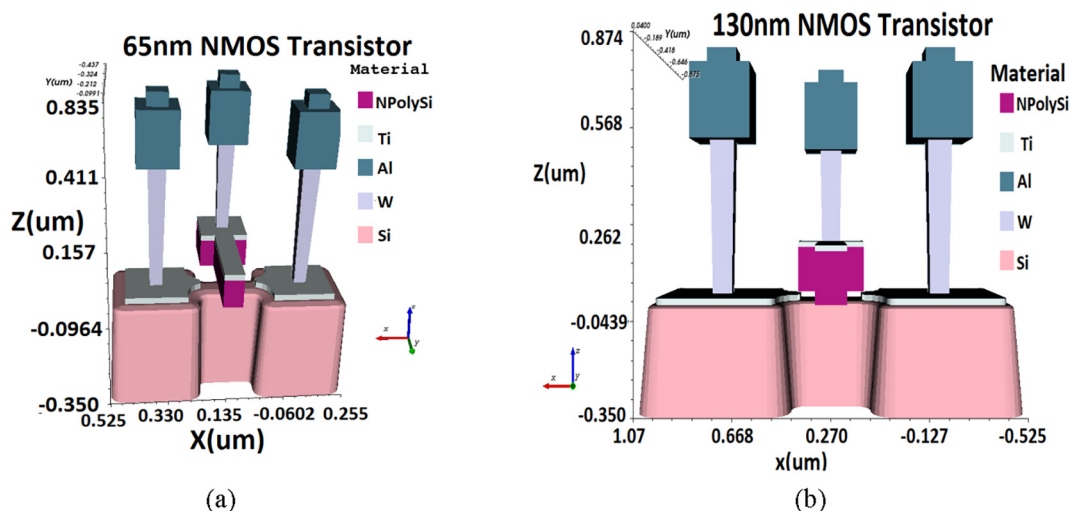


Fig. 3. TCAD models of analyzed NMOS devices designed in (a) 65 nm and (b) 130 nm technology.

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