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Anomalous annealing of floating gate errors due to heavy ion irradiation

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ABSTRACT

Using the heavy ions provided by the Heavy Ion Research Facility in Lanzhou (HIRFL), the annealing of heavy-ion induced floating gate (FG) errors in 34 nm and 25 nm NAND Flash memories has been studied. The single event upset (SEU) cross section of FG and the evolution of the errors after irradiation depending on the ion linear energy transfer (LET) values, data pattern and feature size of the device are presented. Different rates of annealing for different ion LET and different pattern are observed in 34 nm and 25 nm memories. The variation of the percentage of different error patterns in 34 nm and 25 nm memories with annealing time shows that the annealing of FG errors induced by heavy-ion in memories will mainly take place in the cells directly hit under low LET ion exposure and other cells affected by heavy ions when the ion LET is higher. The influence of Multiple Cell Upsets (MCUs) on the annealing of FG errors is analyzed. MCUs with high error multiplicity which account for the majority of the errors can induce a large percentage of annealed errors.

1. Introduction

Flash memories are the most popular non-volatile memories on the semiconductor market. Unlike SRAM, a Flash memory cell is a floating gate MOS transistor. The amount of charge stored in FG determines the data of cell. Flash memories have been widely used in many space systems due to their high density and non-volatility [1]. However, they are not immune to radiation effects. The single event effect (SEE) and total ionizing dose (TID) can threaten their operation and service life seriously in radiation environment. For this reason, more information on their SEE and TID susceptibility is needed before they can be used in harsh environments.

Many studies have been published on the SEE and TID of Flash memories during the last decades [2–8]. As far as the radiation effects were concerned, one single ion could not cause the error in FG [2,3]. The most sensitive part in Flash memories was the peripheral circuitry. With the scaling of technology, the amount of charge stored in FG cells was reduced continuously, which caused the read margin to become smaller and increased the cell sensitivity. Finally, the errors in FG cells were discovered [4]. Now the FG array becomes more and more sensitive to radiation [8–10].

Some mechanisms have been proposed to explain the FG errors: charge loss from the FG due to a transient conductive path across the tunnel oxide [11] or the transient carrier flux over the oxide barriers [12]; and charge trapping in the tunnel oxide [13,14]. Due to the non-volatility, the data in FG cell will not be lost without power under normal conditions. However, the information stored in FG cells could change with time after heavy ion irradiation. When one heavy ion hits the FG cell, the threshold voltage (V_{th}) shift induced by charge loss ($\Delta V_{th,CL}$) and charge trapping ($\Delta V_{th,CT}$) makes the programmed cell ('0') V_{th} shift. If the shift is large enough so that V_{th} becomes lower than the read voltage (V_{read}), a cell error occurs. The discharge induced by charge loss is permanent without reprogramming, but the charge trapping could be recovered over time. Depending on the contributions of $\Delta V_{th,CL}$ and $\Delta V_{th,CT}$, the error may anneal or not after irradiation. If $\Delta V_{th,CL}$ alone is needed to cause the error, the error will not anneal. On the contrary, if both $\Delta V_{th,CL}$ and $\Delta V_{th,CT}$ are needed to bring cell V_{th} beyond V_{read}, owing to charge neutralization the cell V_{th} may pass V_{read}, which leads the annealing of the cell error [15]. The annealing of FG errors should be taken into account. Because neglecting the annealing effect may cause an overestimation or underestimation on the number of errors in some situations [16]. The annealing of heavy-ion induced FG errors has been reported in the literature [13–15,17]. However, as we know, the annealing of heavy-ion induced FG errors with the ion LET higher than 65 MeV·cm^2/mg has not been reported yet.

In this paper, the annealing of FG errors in 34 nm and 25 nm NAND flash memories irradiated by heavy ions with different LET is presented. The dependence of annealed errors on the ion LET, device feature size

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Table 1
Micron technology nand flash memories under study.

Part Number	Density [Gb]	Date Code	Feature Size [nm]
MT29F1G08ABADA	1	1340	34
MT29F16G08ABACA	16	1446	25

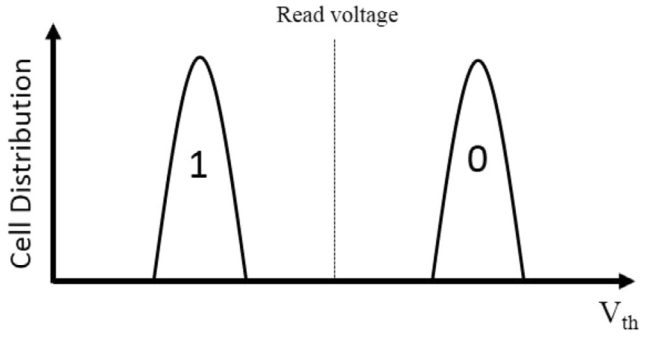

Fig. 1. The sketch for V_{th} distribution in SLC Flash memories.

Table 2
The parameters of heavy ions used in the experiments.

Ion	Ion energy at device surface [MeV]	Ion LET at device surface [MeV·cm^2/mg]	Ion range in silicon [μm]
^{86}Kr	1818.1	20.7	268.7
^{86}Kr	1007.5	29.1	92.4
^{86}Kr	479.8	37.6	58.5
^{129}Xe	1932.7	50.3	145.2
^{129}Xe	711.0	67.1	54.1
^{209}Bi	923.2	99.8	53.7

and data pattern is analyzed. Through the variation of the percentage of different error patterns in 34 nm and 25 nm memories with annealing time, the annealing of FG error is located. The experimental phenomena are explained by the shift of the cell threshold voltage.

2. Experimental details

2.1. Devices under test (DUTs)

In the experiments, we studied the commercial Single Level Cell (SLC) NAND Flash devices manufactured by Micron Technology: 1 Gb 34 nm and 16 Gb 25 nm Flash. The details of the devices are summarized in Table 1. The sketch of SLC Flash cell threshold voltage (V_{th}) distribution is shown in Fig. 1. By changing the amount of charge in FG cell, the threshold voltage (V_{th}) of the memory cell is modified. The FG cell is a special type of MOSFET with a programmable threshold voltage depending on the amount of trapped charge in the FG. The SLC memories store 1 bit per cell, when the read voltage is higher than the cell V_{th}, the cell is on ('1'), otherwise it is off ('0').

2.2. Experiment setup

The memories were irradiated at the Heavy Ion Research Facility in Lanzhou (HIRFL). Three kinds of heavy ions (^{86}Kr, ^{129}Xe and ^{209}Bi) were used to irradiate the Flash memories and the Al degraders with different thicknesses were used to obtain different energy in order to change the ion LET. The parameters of ions used in the experiments calculated by SRIM 2013 code [18,19] are listed in Table 2.

All the tests were carried out in air at room temperature with normal incident beam. The DUTs were etched to remove the plastic package and NAND Flash blocks were programmed with different patterns (all '0', checkerboard '55' or anti-checkerboard 'AA') prior to

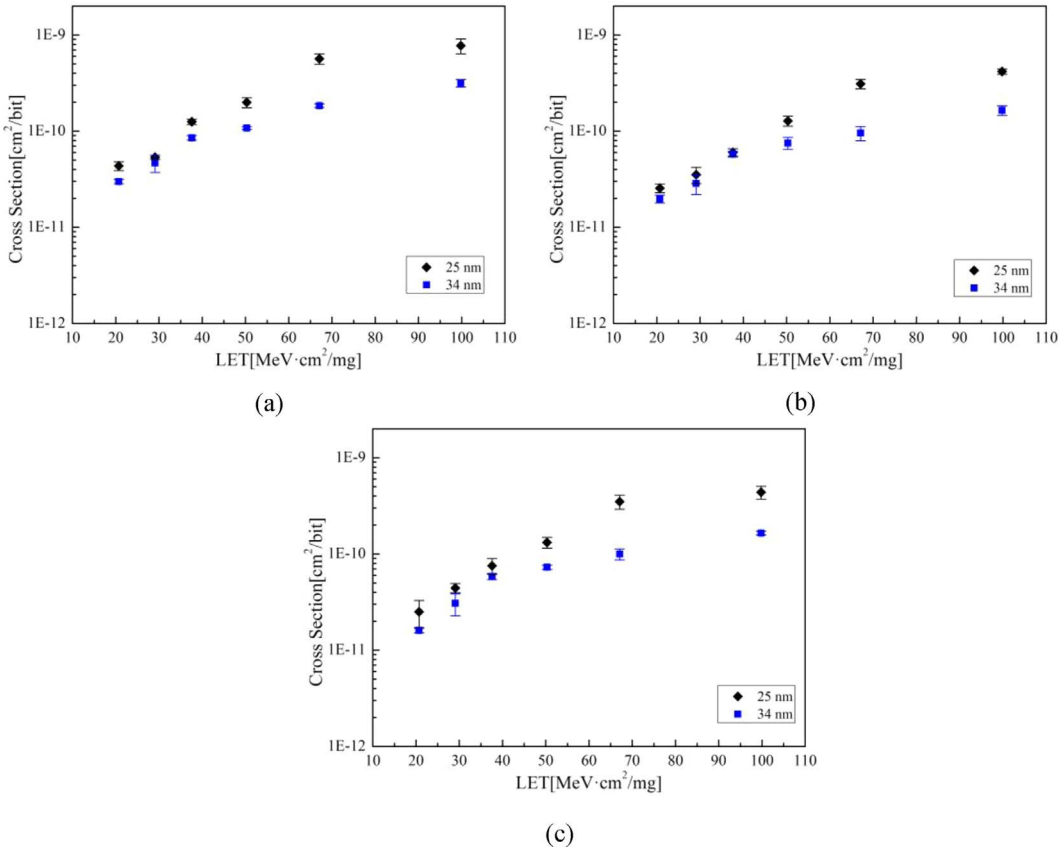

Fig. 2. The FG SEU cross section for Micron Technology 34 nm and 25 nm SLC NAND flash memories. (a): The blocks were programmed with all '0'; (b): The blocks were programmed with checkboard '55'; (c): The blocks were programmed with anti-checkboard 'AA'.