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Swift heavy ion irradiation induced electrical degradation in deca-nanometer MOSFETs

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ABSTRACT

In this work, degradation of the electrical characteristics of 65 nm nMOSFETs under swift heavy ion irradiation is investigated. It was found that a heavy ion can generate a localized region of physical damage (ion latent track) in the gate oxide. This is the likely cause for the increased gate leakage current and soft breakdown (SBD) then hard breakdown (HBD) of the gate oxide. Except in the case of HBD, the devices retain their functionality but with degraded transconductance. The degraded gate oxide exhibits early breakdown behavior compatible with the model of defect generation and percolation path formation in the percolation model.

1. Introduction

As CMOS technology advances to the deca-nanometer nodes, the inherent tolerance to ionizing radiation of these advanced MOSFETs has attracted much interest in the development of integrated circuits capable of withstanding very high ionizing radiation doses, beyond 100 Mrad (Si). It is well known that the single-event effect (SEE) is the predominant concern for nanometer MOSFET transistors operating in an environment with radiation [1–3]. On the other hand, the total ionizing dose effect (TID) is considered relatively negligible in the ultra-thin gate insulator (<3 nm) utilized in these transistors [4]. It has been reported that the electrical characteristics of MOSFETs in a 65 nm CMOS device are relatively stable after being exposed to X-ray or proton irradiation with ionizing doses of greater than 100Mrad [5,6].

These studies have been focused on X-ray, gamma and proton irradiation, which employ the standard test procedures for TID and displacement damage (DD) effects. However, there are few publications on the effect of heavy ion irradiation on nanometer MOSFETs.

In addition, it is commonly known that swift heavy ions (SHI), when penetrating a solid, lose their energy predominately through inelastic interactions with the target electrons. The resulting intense electronic excitation can produce a narrow trail of permanent damage along the ion path, also known as an ion latent track [7–11]. Previous studies have shown that a high fluence of heavy ions caused increases in leakage current across the ultra-thin SiO_2 gate insulator in MOS capacitors. This is referred to as the radiation induced leakage current (RILC) [12,13]. Also the level of the damage increases with the number of the impacting ions [14]. Despite these studies, the effect of SHI on MOSFETs has not been thoroughly investigated.

In this work, the effect of swift heavy ion irradiation on MOSFETs from a commercial 65 nm CMOS technology is studied. This particular technology has been a popular choice for use in radiation tolerant circuitry developed for aerospace and accelerator applications. The observed degradation of both the electrical characteristics and physical structure of the MOSFETs is reported here.

2. Device structure and experiment setup

The transistors were fabricated on a commercial low-leakage 65 nm CMOS device baseline and only the core nMOSFET transistors were investigated in this study. The minimal channel length of the core device is 60 nm. The gate stack consists of a silicon-oxynitride insulator and poly-crystalline silicon electrode. The equivalent oxide thickness (EOT) of the gate insulator is 2.35 nm. The samples were bare dies without packaging. There was approximately 10 μm of additional dielectric and metal interconnect over-layers above the active transistors.

Heavy ion irradiation experiments were performed at the Heavy Ion Research Facility (HIRFL) in the Institute of Modern Physics, Chinese Academy of Sciences, Lanzhou. A 2150 MeV $^{86}Kr^{26+}$ ion beam was used to irradiate the samples in the direction normal

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to the sample. In this experiment, there were 120 samples irradiated. Three independent experiments were performed with fluences of 1 × 10^{10} ions/cm^2, 1 × 10^{11} ions/cm^2 and 1 × 10^{12} ions/cm^2. All terminals of the transistors were electrically floating during the irradiation. The Linear Energy Transfer (LET) value near the gate insulator was 19. At the highest fluence, the ionizing dose near the MOSFET channel was 3.0 × 10^6 Gy (Si).

The DC characteristics of the as fabricated and irradiated sample were measured by an Agilent 4156C semiconductor parametric analyzer with the source and body terminal grounded. The transfer characteristics (I_d–V_g), output characteristics (I_d–V_d), and gate leakage current (I_g–V_g) of the transistors were measured. The uniformity of the operation of devices was checked by first measuring 60 devices before irradiating.

As there was no significant difference in the behavior of these devices it is reasonable to take one of these typical curves as the behavior before irradiation. The same methodology was applied to the measurements of the irradiated samples. So 40 devices (20 tested samples and 20 fresh samples) were irradiated independently for each fluence. Some transistors were subjected to accelerated constant voltage time dependent dielectric breakdown (TDDB) tests under high electric field. The morphology of the cross sections of the gate stack, before and after Kr ion irradiation, was studied using a Transmission Electron Microscope (TEM).

3. Results and discussion

As mentioned the MOSFETs were subjected to various fluences of Kr ion irradiation and the electrical characteristics were studied. The first key point to note is that the transistors remain functional even after the high fluence of Kr ion irradiation, thus it is possible to perform all the required electrical measurements. Fig. 1a shows the drain current as a function of the gate voltage for both the as-fabricated and the irradiated MOSFETs. The threshold voltage can be determined for all three fluences and can be compared to that of the non-irradiated MOSFET. The values are 0.52 V, 0.53 V, 0.51 V, 0.53 V for the non-irradiated and 1 × 10^{10} ions/cm^2, 1 × 10^{11} ions/cm^2 and 1 × 10^{12} ions/cm^2 fluence, respectively. From these values, it is immediately clear that the shift of the threshold voltage is 10 mV, −10 mV and 10 mV after the three flurences, respectively. So the difference between them is only 20 mV and thus almost negligible within errors. This behavior of the threshold voltage shift is similar to that in a recent report in which 65 nm MOSFETs were exposed to proton and X-ray irradiation with an ionizing dose of up to 10^7 Gy(SiO$_2$) [6]. In our case, the dielectric property of the gate insulator seemed to remain intact and the charge trapping in the gate dielectric is minimal.

Fig. 1b also shows the gate current as a function of the gate voltage for the non- and three fluences irradiated MOSFETs. It is clear that there is a significant effect from the irradiation on the gate current in the region of negative gate bias. In fact the gate current is increased by two orders of magnitude for the highest fluence. One possible reason of this increase may be the consequence of an increased gate leakage current flowing from the drain to the gate. This would imply that there is a degradation of the insulation properties in the SiON dielectric. Another possible reason may be the source-drain current of the parasitic MOSFET at the shallow trench isolation (STI) sidewall. However, this very unlikely as the doping concentration in the active region is high enough such that the positive charges trapped in the oxide are not of sufficient concentration to give rise to parasitic capacitance.

The transconductance (g_m) is shown in Fig. 1c as a function of the gate voltage for all the irradiation cases. It shows clearly that there is a sizable decrease in the peak transconductance with the high fluence of heavy ions. Hence this strongly suggests that there is noticeable degradation of the transistor. This would be expected if the ion irradiation were to generate traps from a roughened Si/SiO$_2$ interface along the latent track. The charge carriers in the channel may then experience Coulomb scattering resulting in a decreased mobility and thus decreased transconductance.

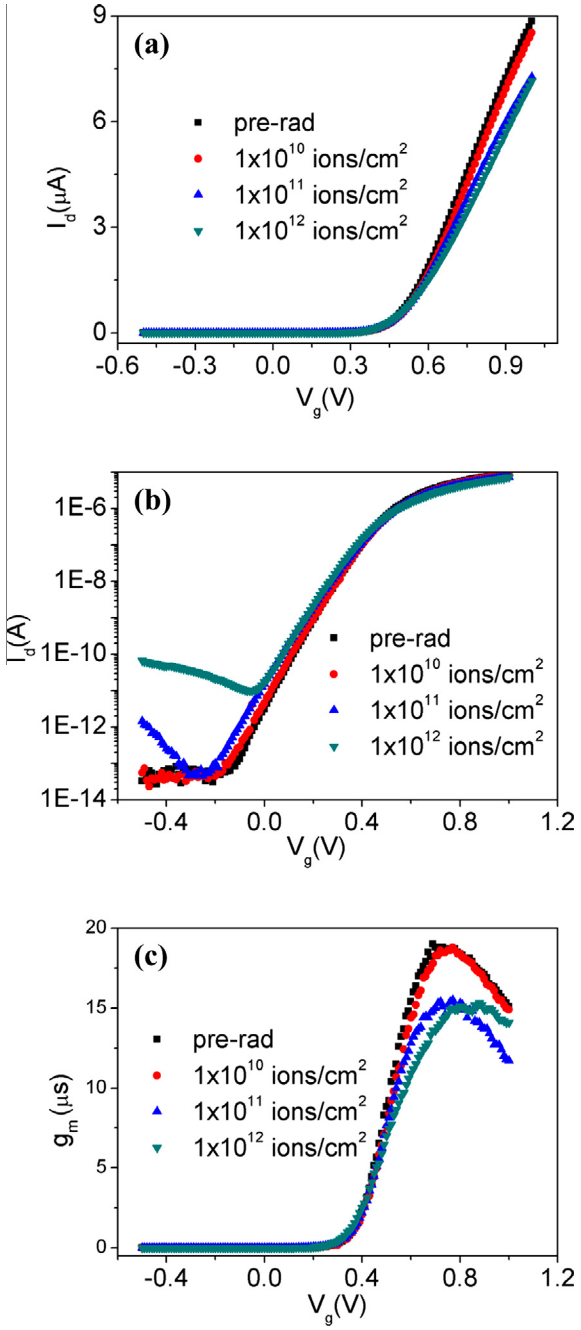

Fig. 1. I_d–V_g curves of the minimum-size transistor (W/L = 120/60 nm) before and after Kr-ion irradiation. The irradiation fluence was 1 × 10^{10} ions/cm^2, 1 × 10^{11} ions/cm^2, and 1 × 10^{12} ions/cm^2.

In order to study the leakage current further, the I_g–V_g characteristics were measured for the MOSFETs after the various fluences. The results are plotted in Fig. 2. The overall trend is that the leakage current grows with increasing fluence, although the behavior varies among different transistors. The behavior can be understood in the following way. The I_g–V_g curve under low fluence first exhibits standard-induced leakage current (SILC)-like characteristics increasing from the non-irradiated value by an order of magnitude.