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System on chip (SoC) microcontrollers (μC) as digitisers for ion beam analysis (IBA) instruments ☆

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ABSTRACT

Data digitisation of the analogue signals from detectors to digital data is an essential process in ion beam analysis (IBA). The low-cost, easy availability and development environments that have a low learning threshold makes system-on-chip (SoC) microcontrollers (μC) attractive for this task. These μC combine, on one die, analogue and digital inputs and outputs with serial USB interfaces, which opens up simple implementation of tailor-made interfaces for specific IBA measurement systems. We have investigated the design and performance limitations based on development of three different digitisation interfaces for IBA. These were a two-channel nuclear instrumentation module (NIM) ADC event mode interface (EMI) for a high-resolution magnetic RBS spectrometer, a simple headless-multi-channel analyser (MCA) and a combined dual channel headless MCA and EMI. It is shown that SoC μC based interfaces for digitisation of analogue spectroscopy pulses in IBA systems can be implemented for material costs less than 100 €. The performance of the SoC devices for many IBA applications is close to what can be achieved with state-of-the-art instruments. The simple pulse spectroscopy interface circuit and software are included in the auxiliary archive.

1. Introduction

Many ion beam analysis (IBA) measurements employ similar electronics readout chains. The most common is conventional analogue pulse electronics [1,2] with a pulse-height digitising analogue to digital converter (ADC) feeding a computer for data presentation and storage. Often digitisers are implemented in the standard Nuclear Instrumentation Modules (NIM) [3] which is expensive, heavy (~17 kg per crate) and power consuming (5–20 W per slot) although more compact externally powered units are becoming available. Direct digitisation of the pre-amplifier signal by a digital signal processor (DSP) with using digital filtering is emerging as an alternative, particularly for high counting rates. The cost per channel for these approaches is approximately the same. The DSP approach has several drawbacks. (i) Maintaining synchronicity between DSP modules for read-out of many channels in event mode can be difficult. (ii) Important details about how the pulses are processed, which may influence the results and the device interfacing, may be proprietary information that is not available to the user, or cannot be re-configured for customisation because they are implemented in firmware. (iii) Non-standard proprietary interfaces can also lead to obsolescence problems with change of the host computer or operating system. More advanced programmable pulse digitiser and DSP systems may be based on field programmable gate array (FPGA) systems, e.g. Ref. [4]. Making full-use of the potential of these flexible and higher performance advanced systems requires extensive programming skills. This is a drawback because it gives a high learning threshold for these flexible instruments.

System on chip (SoC) microcontrollers (μC) with a USB interfaces have become readily available at low cost [5–7]. These SoC have an on-chip processor, flash and dynamic memory as well as peripheral digital input/output (i/o) and serial/USB interfaces, analogue to digital converters (ADC) and digital to analogue converters (DAC) [5,6]. SoCs allow a dramatic reduction in component numbers and internal wiring complexity compared with conventional ADCs/digitisers. This is significant because it reduces cost, simplifies construction and fault-finding. Furthermore, less internal wiring improves reliability. The use of open source SoC μC hardware and software and a standard USB serial class interfacing facilitates modification, reconfiguration and repair by the user and reduces obsolescence problems. The low, learning thresholds for programming, cost and power (~0.1 W, supplied via the USB interface) makes SoC μC interesting for users to tailor-make instruments

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with built-in pulse spectroscopy capabilities, [8] (e.g. for automatic channelling measurements). This is a more flexible approach and reduces reliance on shared central laboratory data acquisition systems.

Here, the performance and implementation of several low-cost pulse-height digitising instruments for IBA are presented. (i) A two-channel event mode interface (EMI) for a magnetic Rutherford backscattering spectrometry (RBS) spectrometer that reads-out legacy NIM ADCs. (ii) A headless multi-channel analyser (MCA) for Si detectors. (iii) A two channel EMI and MCA for Time of Flight-Energy Elastic Recoil Detection (ToF-E ERDA). The materials costs for each of these instruments was less than 100 €. The difference between a MCA and a EMI interface is that in the former, the contents of the address in the buffer corresponding to the ADC conversion values are histogramed to create a 1D pulse height spectrum, while in the EMI case; the sets of ADC conversion values themselves are stored as tuple records in the buffer which are subsequently sorted by the host computer to generate 1D and multidimensional histograms. In Time of Flight – Energy Elastic Recoil Detection Analysis (ToF-E ERDA) an EMI with pair of ADCs is used to measure the 2D energy detector and time spectra. The Arduino open source platform [5] was chosen because of, low cost, low learning threshold and a real-time environment without ill-defined operating system latencies. Software and an accompanying technical note describing a practical generic interface circuit [9] are deposited in the auxiliary archive.

1.1. Pulse spectroscopy requirements for IBA

The specific characteristics of IBA pulse spectroscopy measurements are: (i) Series of samples are often measured with automated settings. (ii) Usually only a single, or a few detectors in coincidence are used. E.g. ToF-E ERDA, (iii) The pulse spectroscopy system and other components used are connected to a PC which performs display and data storage functions. (iv) The relative energy resolution ($\Delta E_{fwhm}/E$) does not exceed 0.05–0.1% for standard Si X-ray and charged-particle detectors. For standard ToF-E ERDA with 0.05–0.5 MeV/u recoil energies and 250 ps FWHM time resolution, the flight times are 50–160 ns over 0.5 m. This implies digitisation with more than 1024 or 2048 channels resolution is not meaningful. (v) Dead-time associated spectrum distortion is detrimental for the quantitativeness and sensitivity of IBA measurements. (vi) The accuracy may be degraded by differential and integral non linearities in pulse height conversion.

Special consideration needs to be given to dead-times which restrict system throughput. Dead-time can be characterised as paralysed, τ_P, and non-paralysed, τ_{NP}, dead-time [1]. τ_P gives a loss of registered pulses $p_P = \tau_P f$, where f is the mean pulse rate. A trivial correction of p_P can be applied for quantitative IBA applications. τ_{NP} is more problematic because if two pulses occur within τ_{NP}, they are treated as a single composite pulse giving pulse pile-up, which in IBA limits the instrument detection level (IDL) for PIXE and RBS analysis of trace elements. The pile-up probability is, $p_{PU} = (1 - e^{-f\tau_{NP}})$ [1]. For a fast ADC with negligible conversion time, the τ_{NP} and τ_P are governed by the duration of the pulse at the ADC input. For a semi-Gaussian pulses with 3 μs pulse peaking time at $f = 1000$ pulses s^{-1}, p_P = 0.83% and p_{PU} = 0.3%. (Fast ComTec 7072 dual fast ADC [15], Table 1.) These losses increase with increasing f, with p_P and p_{PU} reaching ~4.2% and ~1.5%, respectively at $f = 5000$ pulses s^{-1}.

1.2. Basic μC interface considerations

In both MCA and EMI interfaces, two processes must take place concurrently. Firstly, the ADC(s) must be read out at random times and the ADC data stored in a buffer. Secondly, the EMI and MCA buffer(s) must be read out to the host. Service functions, (start-stop ADCs, zero buffers, set threshold and delays etc.) must also be performed. This situation lends itself to a program structure based on a two concurrent autonomous threads. One thread reads out the ADC and stores data in the buffer under interrupt control and the other sequentially performs service functions such as serial readout under host control. This two-thread approach was adopted because it is easy to implement and can make a more efficient use of processor time than other possible structures, such as a hierarchical state machine. Where both threads share a single processor, the maximum throughput is set by the requirement that the time taken to process a single event must be less than $1/f$.

The interrupt driven ADC service thread performs coincidence checks, reads the ADC(s) and writes the data to the output buffer (s), increments counters and finally resets the ADC interface [9]. The readout thread is simply a polling loop that interrogates the incoming serial port for commands such as binary read out of buffer contents, start/stop/zero etc. If any commands are found the appropriate thread is branched to.

2. Two-NIM ADC event mode interface (EMI)

A system for event mode readout of a pair of 13-bit legacy NIM ADCs [10] was developed. These are used to digitise the position $P = L/(L + R)$ and total charge $C = (L + R)$ analogue signals from a charge division multi-channel plate focal plane detector on a mag-

Table 1
Digitiser performance comparison.

ADC type and interface	Input chan.	$\tau_P/\mu s$	$\tau_{NP}/\mu s$	Para. loss (1000 s^{-1})	Pile-up (1000 s^{-1})	USB rate[2]/events s^{-1}	Rel. speed[3]	σ/chan	δ BSL[4] % full span
NIM MCA [10]	1	19.1[1,2]	8.9	1.9%	0.89%	5400	1.00		not spec.
NIM EMI [10]	2	29.4[1,2]	8.9	2.9%	0.89%	2700	0.7		not spec.
Simple 10-bit MCA	1	125	20	12.5%	2.0%	5500	0.15	<1.2[5]	−0.1–0.2[5]
12-bit dual MCA	1	8.3[6]	5.8[6]	0.83%	0.58%	11000	1.3	1.5	−0.2–0.6[5]
12-bit EMI	2	9.62	7.8[2]	0.96%	0.58%	5400	1.3	1.5	−0.2–0.6[5]
7070 ADC [14]	1	17.9[7]	3.0[6]	1.8%	0.30%				
7072 ADC [15]	1	8.3[6]	3.0[6]	0.83%	0.30%			<1.7[9]	
DSA-1000 DSP [16]	1	3.7[8]	0.04	0.75%	0.005%[9]				

[1] No buffering, 2048 channels, 50% max span.
[2] At max USB Baud rate.
[3] Relative throughput to NIM MCA with Canberra 8713 ADC [10].
[4] p.–p. deviation from Best Straight Line (BSL).
[5] Over 15–90% of max span.
[6] Limited by input pulse peaking time and duration.
[7] For 12-bit operation.
[8] Trapezoidal shaping 2.6 μs rise/fall time, 0.6 μs flat-top. These are the closest preset values that correspond to a Semi-gassian pulse with 3 μs peaking time.
[9] For 4096 channels.

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