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Time-dependent dielectric breakdown of recessed AlGaN/GaN-on-Si MOS-HFETs with PECVD SiO_2 gate oxide

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ABSTRACT

This paper reports the first-time evaluation of the time-dependent dielectric breakdown of recessed AlGaN/GaN-on-Si metal-oxide-semiconductor heterostructure field-effect transistors (MOS-HFETs) with plasma enhanced chemical vapor deposition (PECVD) SiO_2 gate oxide. The interface fixed charge density and oxide bulk charge density extracted from the flat-band voltage characteristics were $2.7 \times 10^{11} \pm 6.54 \times 10^{10}\,cm^{-2}$ and $-9.71 \times 10^{17} \pm 5.18 \times 10^{16}\,cm^{-3}$, respectively. The time dependent dielectric breakdown (TDDB) characteristics exhibited longer lifetime estimation as the SiO_2 thickness increased. The excellent reliability of the PECVD SiO_2 film was validated for use as the gate oxide of recessed AlGaN/GaN MOS-HFET.

1. Introduction

Over the past few decades, III-nitride heterostructure semiconductors have received great attention owing to their promising material properties and have been commercialized successfully in both optical and electronic applications, such as light emitting diodes, high frequency amplifiers, and fast power switching devices [1–3]. At the electronic device point of view, the strong polarization characteristics of AlGaN/GaN heterostructures result in high electron concentration in the two-dimensional electron gas channel formed at the interface between AlGaN and GaN [4]. Such strong polarization effects render it difficult to achieve the enhancement mode operation of AlGaN/GaN heterostructure field-effect transistors (HFETs) that is required in power switching applications.

The enhancement mode GaN switching FETs available in the market typically employ a p-type (Al)GaN gate structure whose threshold voltage is typically ≤ 1 V [5–7]. An alternative enhancement mode configuration would be a recessed metal-oxide-semiconductor (MOS) structure [8–10] that has benefits of low leakage current and easy controllability of the threshold voltage. The important technical issues of the recessed MOS configuration are the interface engineering and the quality of the MOS gate. In particular, the interface and oxide bulk charges have a significant influence on the threshold voltage and thus device reliability [11,12]. While the trapping phenomena near the MOS interface are responsible for the dynamic switching characteristics, the long-term reliability cannot be directly evaluated by the dynamic switching characteristics. Therefore, it is very important to study the interface and bulk characteristics of gate oxides and their effects on device reliability. Several studies have been reported on GaN-based MOS-HFETs with in-situ SiN_x [13] and various atomic layer deposition films such as Al_2O_3 [14–16], AlO_xN_y [17], and the HfO_2/Al_2O_3 bilayer [18]. To the best of our knowledge, however, none have reported plasma-enhanced chemical vapor deposition (PECVD) SiO_2 that is an excellent candidate for the gate oxide owing to its larger conduction band offset and high breakdown field. Since GaN has a wide energy bandgap (~3.45 eV) and a high breakdown field (~3 MV/cm), great attention has to be paid to the gate dielectric material for GaN FETs that must have a high breakdown field with a large conduction band offset from GaN, low interface and oxide bulk trap densities, and strong durability. In particular, the high breakdown field with a large conduction band offset can suppress the gate leakage current and improve the long-term reliability.

In this study, we have investigated the interface fixed charge density and the oxide bulk charge density of PECVD SiO_2 films deposited on the recessed GaN surface. In addition, the time-dependent dielectric breakdown (TDDB) characteristics of the recessed AlGaN/GaN MOS-HFETs with different SiO_2 gate oxide thicknesses were measured to obtain the correlation between the SiO_2 thickness and device reliability.

2. Experimental details

Wurtzite AlGaN/GaN epitaxial layers used in this work consisted of a 10-nm in-situ SiN_x passivation layer, a 3.8-nm GaN capping layer, a 22.1-nm $Al_{0.23}Ga_{0.77}N$ barrier layer, a 490-nm i-GaN layer, and a 4.45-

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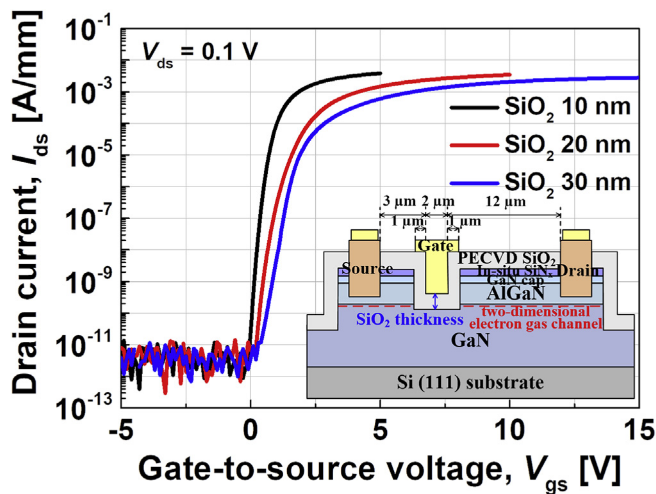

Fig. 1. Transfer characteristics of fabricated devices with various SiO_2 thicknesses at V_{ds} = 0.1 V. The inset is the cross-sectional schematic of the device.

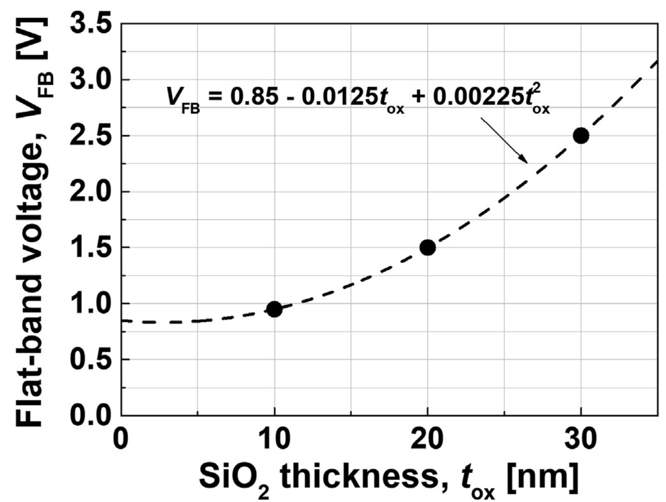

Fig. 3. Extracted flat-band voltage characteristics of metal/PECVD SiO_2/recessed GaN MOS devices.

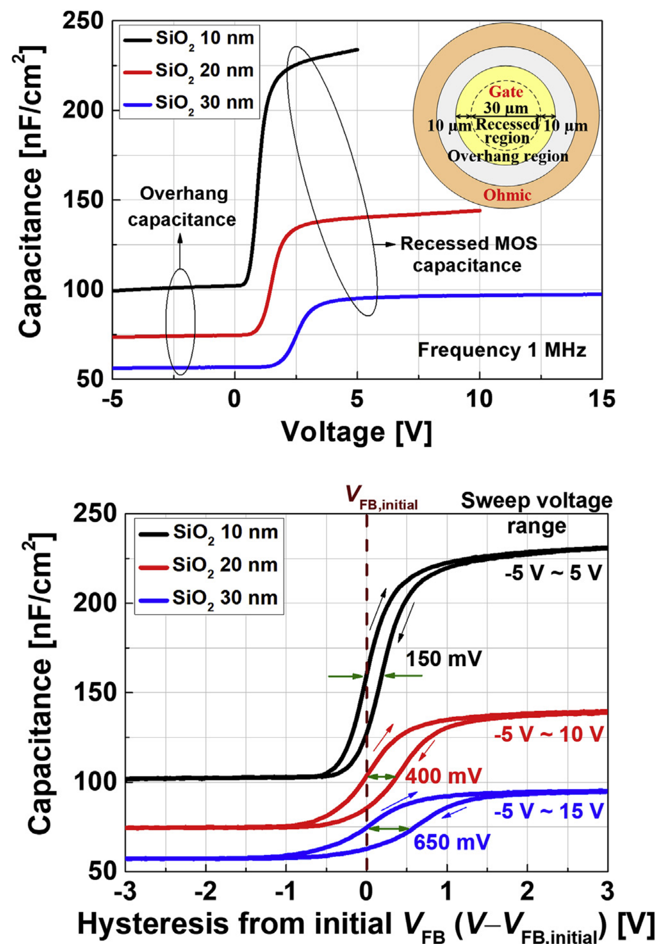

Fig. 2. (a) Capacitance–voltage characteristics of recessed MOS devices with various SiO_2 thicknesses. The inset is the top view schematic of the MOS device. (b) Hysteresis of flat-band voltage relative to the initial values for different SiO_2 thicknesses.

µm GaN buffer layer on Si (111) substrate. The epitaxial wafer was produced by a commercial wafer supplier using metal-organic chemical vapor deposition. First, the source and drain regions were etched by ~15 nm from the GaN surface using Cl_2/BCl_3-based inductively coupled plasma reactive ion etching (ICP-RIE), leaving the remaining AlGaN barrier layer of ~11 nm. Then, a Ti/Al/Ni/Au Ohmic metal stack was evaporated without an additional lithography step, which was annealed at 820 °C for 30 s in a nitrogen ambient [19]. Mesa isolation was also conducted by Cl_2/BCl_3-based ICP-RIE. The measured Ohmic contact resistance was 0.9 Ω mm with a sheet resistance of 463 Ω/sq. After patterning the gate region, the exposed in-situ SiN_x film was etched away using SF_6 plasma etching followed by the gate recess process using low-power Cl_2/BCl_3-based ICP-RIE (RF power = 5 W) in order to minimize the plasma induced damage on the MOS channel. The etch rate was ~1 Å/s and the recess depth from the surface was ~30 nm corresponding to ~4 nm over-etch under the AlGaN barrier layer. Prior to the gate oxide deposition, the wafer was solvent cleaned and dipped in a diluted HF (10:1) solution to remove the native oxide, which rarely etched the in-situ SiN_x layer at the surface. The SiO_2 gate oxide films were deposited at 350 °C with SiH_4 and N_2O gas mixtures using PECVD with an RF power of 100 W and a chamber pressure of 2 Torr [20]. The gas flow rates of SiH_4 and N_2O were 27 and 540 sccm, respectively. Three samples were prepared with different SiO_2 thicknesses: 10, 20, and 30 nm. A Mo/Au metal stack was evaporated for the gate formation. Finally, post-metallization annealing was carried out at 400 °C for 10 min in an O_2 ambient, which was an important process step to improve the interface conditions. The effects of the post-metallization O_2 annealing on SiO_2/GaN interface was reported previously in Ref. [19].

The fabricated devices had a source-to-gate distance of 3 µm, a recessed gate length of 2 µm, a gate-to-drain distance of 12 µm, and a gate width of 100 µm. The overhang length of the gate metal outside the gate recess region was 1 µm in both the source and drain sides.

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