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Electrical stress probing recovery efficiency of 28 nm HK/MG nMOSFETs using decoupled plasma nitridation treatment

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ABSTRACT

Exposing the feasible nitrogen concentration and annealing temperatures with decoupled plasma nitridation (DPN) treatment to the high-k dielectric after deposition as gate dielectric is impressive to raise the high-k value and against the gate leakage. The study not only focuses on the quality of high-k dielectric, but the reliability concern. Using the voltage stress sensing and analyzing the recovery of gate dielectric, comparing with different nitrogen concentration and different annealing temperatures is done. The consequences show the tested device with higher annealing temperature has the better performance rather than the lower one in recovery and drive current, but the worse in reliability stress, especially in threshold voltage (V_T) shift. If the tested devices were under the same nitridation treatment, the performance and recovery efficiency of the tested device with the lower nitrogen concentration are better than those of the higher one, but the degradation rate is more distinct.

1. Introduction

With the shrinkage of device feature size following the Moore's law until 45-nm-node process, the oxide thickness will be less than 1.3 nm [1]. The gate oxide has serious gate leakage current. To solve the gate leakage current and maintain the same equivalent oxide thickness (EOT) [2], it seems that the high-k (HK) dielectric is a feasible candidate. Thus, the HK dielectric materials such as HfO_2 or ZrO_2 incorporating to the nano-node process integration are becoming impressive [3–5]. For the wonderful characteristics of HfO_2 dielectric in k-value, leakage, available incorporation and lifetime operation, this dielectric is indeed a promising high-k gate dielectric candidate compatible with the polysilicon gate process [6].

After the high-k material deposition, using the decoupled plasma nitridation (DPN) is a good choice to fix the oxygen vacancies and bulk traps in this dielectric. This treatment generally promotes the performance of MOSFET devices [7–13]. The integrity of deposited gate dielectric with high-k material under different nitrogen concentration and different annealing temperature will be chiefly studied in this work.

There is leakage current from the gate through the high-K dielectric layer [14–17] and interfacial layer (IL) to the substrate. The interfacial layer material is silicon oxide (SiO_x). Generally, the gate current tunneling mechanisms in SiO_2 dielectric layer can be classified as two parts. First of all, if the gate voltage (V_G) is large enough, the moving electrons see a triangular barrier and the gate current is due to tunneling, called the Fowler-Nordheim (F-N) tunneling. Second, if the oxide layer is very thin and the gate voltage is small, the gate current tunnels through the SiO_2 layer, called the direct tunneling (DT). When the oxide thickness is reduced to less than 4 nm, the direct tunneling gradually becomes dominant. In this study, the interfacial layer thickness is 0.9–1.2 nm, the IL tunneling mechanism is attributed to direct tunneling. The HK dielectric tunneling mechanism is principally attributed to trap-assisted tunneling (TAT) or Poole-Frankel (P-F) tunneling [18–20]. The IL and HK layer tunneling band diagram is

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shown in Fig. 1(a). As the gate is positively biased, the channel carriers tunnel through the interfacial layer by DT, and then tunnel through the high-k layer to form a gate leakage current by TAT. Fig. 1(b) exhibits the tunneling effect at the negative bias condition to the gate and the electrons tunnel through the high-k layer by TAT, and then through the IL by DT [21].

When a dielectric is stressed with the positive bias to the gate terminal, defects will be generated randomly in dielectric. The gate leakage is increased by new random defects, called a stress-induced leakage current (SILC) before the soft breakdown [22,23].

2. Formation of MOSFET devices

The test structures throughout this work are nMOSFETs with 28-nm node high-k/metal gate (HK/MG) stack which were fabricated by UMC. Fig. 2 shows the cross-sectional device structure. After standard cleaning, the interfacial layer was performed. Then, the high-k material was fabricated as sandwiched $HfO_x/ZrO_y/HfO_z$ (HZH) by atomic layer deposition (ALD) technique. In addition, the gate-last (GL) process was employed to form the metal gate and reduce the threshold voltage, gate electrode resistance, power consumption and gate delay. After formation of the high-k layer, the Decoupled Plasma Nitridation (DPN) treatment [8] was applied. The process was with the annealing temperature (600–1000 °C) and the nitrogen concentration (10–20%) conditions after accomplishing high-k layer. Because of reducing the gate leakage through HK layer and increasing the reliability performance of the whole gate dielectric [4,5], the nitrogen treatment to the gate process at annealing step was added. The nitrogen radical is helpful to retard the oxygen vacancy or bulk traps in high-k dielectric. After the gate dielectric stack, the structure of metal gate including bottom barrier metal, work function (WF) metal and top barrier metal and lower resistance metal as a gate electrode was consequently formed. The other back-end-of-line (BEOL) processes follow the standard CMOS process flow until the first metal layer with passivation deposition and pad window opened. The briefly full 28-nm HK/MG process flow with gate-last (GL) process is shown in Fig. 3.

3. Results and discussion

In this work, a process split table of the process conditions for the tested devices is shown in Table 1. The basic electrical characteristics are extracted with Keithley 4200 Semiconductor Characterization System. Table 2 shows the feature size of tested device,

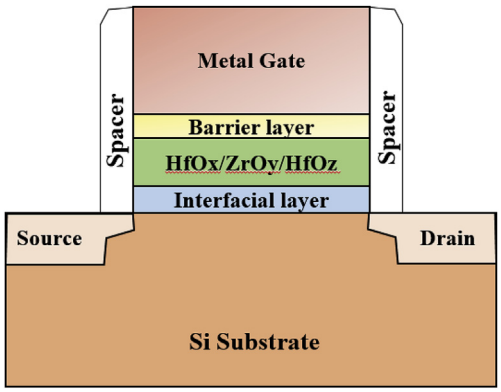

Fig. 2. Schematic profile of a HK/MG MOSFET.

temperature and the experimental conditions. In the beginning, the stress condition was positive voltage $V_G = 1.8V$ as the $V_{CC} = 0.8V$, and the stress time was applied from 0 to 500 s. Next, the tested device was immediately recovered with the reverse stress voltage $V_G = -1.8V$ during 500 s. Finally, we apply a second stress with the same condition as that of the first stress. The experimental principle was to apply stress twice, before-and-after recovery, comparing the two changes of threshold voltage (V_T) and gate current (I_G) in stress to observe the recovery effect of devices in electrical characteristics.

The consequence of the stress is the degradation of threshold voltage as shown in Fig. 4. The higher temperature annealing has the less V_T degradation during stress 1 and 2, and the recovered performance for higher temperature annealing was better than others due to the trap amount recovered more. The least V_T shift after stress and recovery is the higher N_2 concentration sample due to the trap is difficult to be generated. The degradation and recovery of V_T effect show some difference among three tested samples, as shown in Table 3.

However, the higher N_2 concentration sample has the higher V_T at first, and the gate leakage current is higher than others, no matter what was before or after stress. Due to the higher N_2 concentration [24,25], the quality of interfacial layer is possible to decrease, the I_G recorded by time history during stress and recovery tests is shown in Fig. 5. The higher temperature annealing has the lower I_G current due to the higher temperature forming the thicker interfacial layer than the others. Table 4 shows the I_G change with stress and recovery. The gate leakage for sample A and C at the end

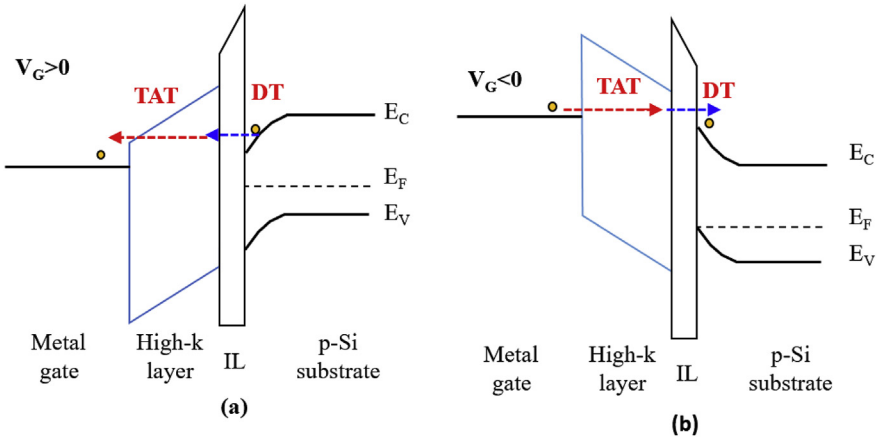

Fig. 1. Band diagram with trap assisted tunneling through high-k layer and interfacial layer of (a) positive gate bias and (b) negative gate bias.