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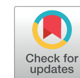
Hard mask and lithographic capabilities improvement by amorphous carbon step coverage optimization in high aspect ratio device pattern



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ABSTRACT

Due to the complexity of micro control unit (MCU), the fabrication process of MCU has become very challenging, and in particular the hard mask (HM) and lithographic technologies. Therefore, it is very important to improve the performance of the two processes. The performances of the HM and lithographic processes strongly depend on the step coverage (S/C) of HM. Poor HM S/C will directly impact the protection provided by HM on device patterning during the etching process and overlay marks during photoresist (PR) rework. The application of C_2H_2 base amorphous carbon (a-C) to form the HM instead of C_3H_6 base a-C can achieve better sidewall and bottom S/C due to the fact that C_2H_2 base a-C has superior sticking coefficient (higher carbon to hydrogen (C/H) ratio). Furthermore, the silicon (Si) center damaging problem in device patterning is alleviated by the good S/C performance of C_2H_2 base a-C. Experimental results have demonstrated that the overlay mark is not damaged with five PR reworks with the application of C_2H_2 base a-C. Furthermore, a process parameter design of experiment (DOE) for C_2H_2 base a-C to obtain the trends of sidewall and bottom S/C is proposed. The presented experimental results show that bad sidewall S/C of a-C film induces the Si edge damage in high aspect ratio device patterning. The proposed DOE will allow us to optimize the C_2H_2 base a-C process to improve the S/C by 49%–91% better than the unoptimized process. This helps to reduce the amount of device pattern damage significantly.

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1. Introduction

Micro control unit (MCU) is widely used in light-emitting diode, appliances, personal computer, mobile device, etc. The different types of memory and logic devices can be embedded in MCU, such as static random-access memory, dynamic random-access memory, electrically erasable programmable read-only memory, and Flash [1–4]. The process of MCU is complex because several memory devices are integrated together. For MCU, one of the key challenges is lithographic process. As the pattern size scaled down to the Sub-100 nm and beyond, etching process becomes more difficult and marginal due to the thin photoresist (PR) of lithographic process [5]. Compared with SiO_2, a hard mask (HM) technology is therefore implemented in lithographic process for the following etching process with a better etching selectivity. Generally, HM is deposited on either a flat area or a low aspect ratio pattern like overlay mark. However, HM is deposited on high aspect ratio pattern (aspect ratio > overlay mark) because of complex process in MCU. The process flow of MCU is given in Fig. 1(a). In our case, two critical processes which are gate and contact definitions need advanced HM technology. For the gate formation of MCU, the film stacking structures of memory and logic devices are different from each other as seen in Fig. 1(b). Hence, the gates of the memory and logic devices are unable to be defined at the same time. Unavoidably, the protection of memory device gate is necessary during the definition of logic device gate. HM is hereby introduced as a protection layer after the definition of memory device gate. Nevertheless, the aspect ratio of memory device pattern in our MCU is 1 (maximum aspect ratio device pattern for HM deposition) which is 10 times larger than the overlay mark used in gate formation. Therefore, it is important to improve step coverage (S/C) of HM.

Regarding the contact definition in MCU, the dimension requirements of device contacts are different in memory and logic devices. The contact of each device is processed individually. Hence, the process of contact is complex. Since HM is deposited on the flat inter-layer dielectric (ILD) to define the contacts in different devices, S/C of HM is insignificant for contact definition. In fact, S/C of HM is still important for the overlay mark of contact formation. Fig. 1(c) provides the film stacking of overlay mark. The overlay

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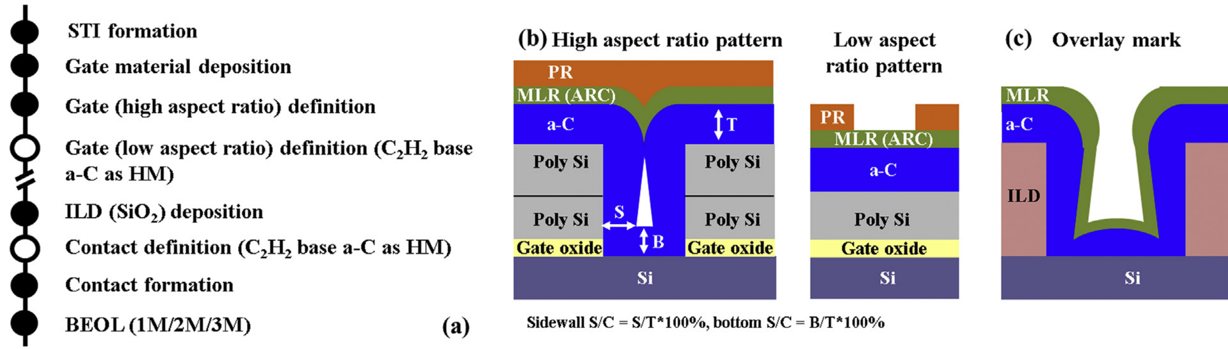


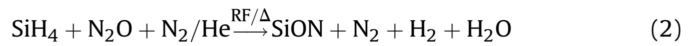
Fig. 1. (a) The process flow of MCU. (b) Film stacking of memory device and logic device during logic device definition. (c) Film stacking of overlay mark in contact definition.

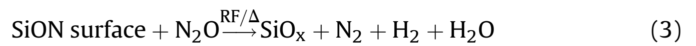
mark has the maximum aspect ratio (0.4) because of thick ILD. Moreover, the process of contact definition has the opportunity for the PR rework of lithographic process. The amount of PR rework would be increased during the contact formation of MCU process. Accordingly, a good S/C of HM is essential for against PR rework. Amorphous carbon (a-C) is popularly used as HM due to its excellent etching selectivity (>10 compared with SiO_2). Furthermore, a-C is widely used in self-aligned double patterning technique to improve the window of lithographic process [6,7]. In this paper, we provide an advanced HM technology to improve S/C of a-C, particularly for side-wall.

2. Experiments

A dual layer stacking is employed that composes of a-C and multi-layer reflection (MLR: SiON + SiOx) with the application of HM and anti-reflection coating by chemical vapor deposition. The tool of a-C deposition is Producer SE from AMAT, and the tool of MLR deposition is Eagle 12 from ASM. Two kinds of precursor of a-C depositon, C_3H_6 and C_2H_2, are carried out, and the reaction equation is as in (1). MLR is used for preventing resist footing problem [8], and the reaction equation is displayed in (2). The N_2O treatment on SiON surface as in reaction equation (3) is implemented to obtain preferable n and k of film properties for following lithographic process, and oxygen (O) radical is produced form N_2O treatment step as shown in reaction equation (4). Without N_2O treatment step, n and k are 2.12 and 1.02, respectively. After 1 day, the n and k decay to 2.08 and 0.7. With N_2O treatment step, n and k are 2.06 and 1, respectively. After 1 day, the n and k keep the same value.

$$C_2H_2/C_3H_6 + He/Ar \xrightarrow{RF/\Delta} C_x + H \quad (1)$$


$$SiH_4 + N_2O + N_2/He \xrightarrow{RF/\Delta} SiON + N_2 + H_2 + H_2O \quad (2)$$


$$SiON\ surface + N_2O \xrightarrow{RF/\Delta} SiO_x + N_2 + H_2 + H_2O \quad (3)$$

$$N_2O \xrightarrow{RF/\Delta} N_2 + O_2 + O^* \quad (4)$$

For the evaluation of HM and lithographic capabilities, four kinds of width size of trench, 0.3 μm, 0.6 μm, 1 μm, and 3 μm with height 0.3 μm in 12 inch wafers are prepared. Overlay mark damage by PR rework is examined in pattern with width 2 μm and height 0.8 μm. In addition, cross-sectional scanning electron microscopy (X-SEM) and optical microscopy (OM) are adopted to check S/C and overlay mark damage performances. Following up, Taguchi method L_{12} (2^7) is used to find the key parameter trend of C_2H_2 base a-C process regarding S/C improvement. Taguchi method is one of powerful design of experiment (DOE) to find out the trend of parameters by using fewer resources. Dr. Taguchi gives many orthogonal arrays base on how many levels and parameters in experiment. Taguchi method L_{12} (2^7) means two levels and seven parameters in experiment. Seven parameters of C_2H_2 base a-C process are investigated as shown in Table 1 in trench with width 0.3 μm and height 0.3 μm. High radio frequency (HRF) power, temperature, and pressure influence the a-C deposition rate. Spacing influences distance between plasma and wafer. C_2H_2 is the main reactant of HM. Argon (Ar) and helium (He) are used for carrier gas of C_2H_2. As regard the root cause of device pattern damage of MCU, cross-sectional transmission electron microscopy (X-TEM) is implemented to point out the position of profile damage. Furthermore, top view SEM is used to calculate the amount of pattern damage of MCU.

Table 1
The DOE of Taguchi method L_{12} (2^7).

Exp.	HRF(W)	Spacing (mm)	C_2H_2(Pa·m³/s)	Ar(Pa·m³/s)	He(Pa·m³/s)	Temperature(K)	Pressure (Pa)
R1	A	B	C	D	E	F	G
R2	A	B	C	D	E	F+100	G+66.7
R3	A	B	C+200	D+1000	E+200	F	G
R4	A	B+2.54	C	D+1000	E+200	F	G+66.7
R5	A	B+2.54	C+200	D	E+200	F+100	G
R6	A	B+2.54	C+200	D+1000	E	F+100	G+66.7
R7	A+100	B	C+200	D+1000	E	F	G+66.7
R8	A+100	B	C+200	D	E+200	F+100	G+66.7
R9	A+100	B	C	D+1000	E+200	F+100	G
R10	A+100	B+2.54	C+200	D	E	F	G
R11	A+100	B+2.54	C	D+1000	E	F+100	G
R12	A+100	B+2.54	C	D	E+200	F	G+66.7

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