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Microstructural, chemical states and electrical properties of Au/CuO/n-InP heterojunction with a cupric oxide interlayer

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ABSTRACT

Cupric oxide (CuO) is synthesized by simple chemical bath deposition method and deposited on n-type InP substrate using e-beam evaporation technique. First, the structural and chemical compositional analysis of CuO/n-InP are analysed by X-ray diffraction (XRD) and X-ray photoelectron spectroscopy (XPS). XRD and XPS results confirmed that the formation of CuO on n-type InP substrate. Then, Au/CuO/n-InP heterojunction is fabricated with a CuO interlayer and correlated its results with the Au/n-InP Schottky junction (SJ). The barrier height (Φ_b) and ideality factor (n) are extracted through I-V and C-V methods and the respective values are 0.66 eV (I-V)/0.80 eV (C-V) and 1.24, and 0.78 eV (I-V)/0.94 eV (C-V) and 1.62 for the SJ and HJ diodes, respectively. By applying Cheung's and Norde functions, the Φ_b, ideality factor and series resistance (R_S) are derived for the SJ and HJ diodes. The derived interface state density (N_{SS}) of HJ is lower than the SJ; results demonstrated that the CuO interlayer plays an important role in the decreased N_{SS}. The Poole-Frenkel emission is the dominant current conduction mechanism in reverse bias of both SJ and HJ diodes.

1. Introduction

Among III-V compound semiconductors, explicitly indium phosphide (InP) has gained considerable interest in the fabrication of electronic and optoelectronic device applications such as high-speed metal-insulator-semiconductor field effect transistors (MISFETs), microwave devices, ultra high-speed integrated circuits (ICs), laser diodes, photo-detectors and solar cells [1–4]. However, the main drawback of the InP Schottky barrier is its relatively low Schottky barrier height (SBH) (0.40–0.45eV); as a result there is large reverse leakage current at the interface [5]. The formation of interlayer between metal and semiconductor is best method to increase the effective barrier. This interlayer can act as a tunnelling barrier [6]. Thus, the formation of interlayer in between the metal and semiconductor and explored its detailed electrical properties are a scientific challenging issue. Some research groups have fabricated and studied the electrical characteristics of metal-interlayer-semiconductor (MIS) structures on Si and n-InP substrate. For instance, Ibrahim et al. [7] prepared Al/CuO/p-Si MIS diode by forming CuO nanofilm with spin coating technique and reported that the barrier height (BH) and ideality factor values were 0.64 eV and 2.39 from I-V characteristics, respectively. Cetinkaya et al. [8] synthesized CuO by chemical bath deposition (CBD) and sol-gel methods, and carried out the structural and electrical properties of Au/CuO/p-Si/Al MIS diodes. Menyawy et al. [9] prepared the Co/n-CuO/p-Si/Al diode and studied its I-V characteristics in the temperature range 300–390 K. Tombak et al. [10] demonstrated that the electrical properties of Ag/CuO/n-Si diode and reported that the BH and ideality factor values were 0.75 eV and 3.51, respectively. Thapaswani et al. [11] presented the electrical parameters of Au/$Ba_{0.6}Sr_{0.4}TiO_3$/n-InP MIS diode increased as compared to the Au/n-InP Schottky junction (SJ) diode. Padma et al. [12] studied the electrical properties of Au/Fe-ZnO/InP MIS structure, and reported that the BH values of MIS structure were increased as compared with that of the Au/n-InP SJ diode. Balaram et al. [13] evaluated the effect of high-k ZrO_2 interlayer between Au and n-InP, and reported that the BH values were enhanced for the

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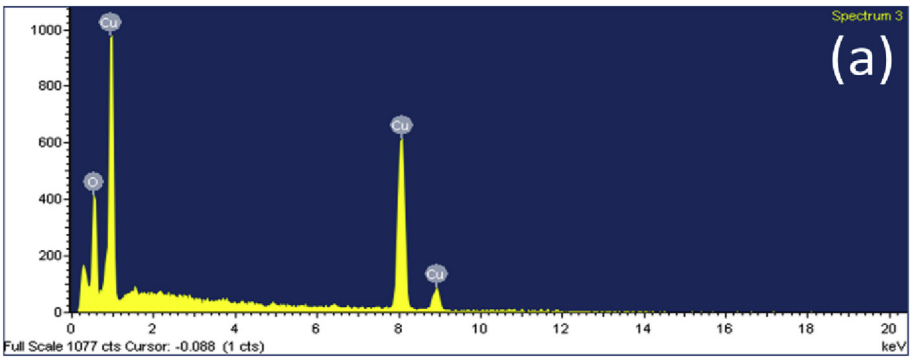
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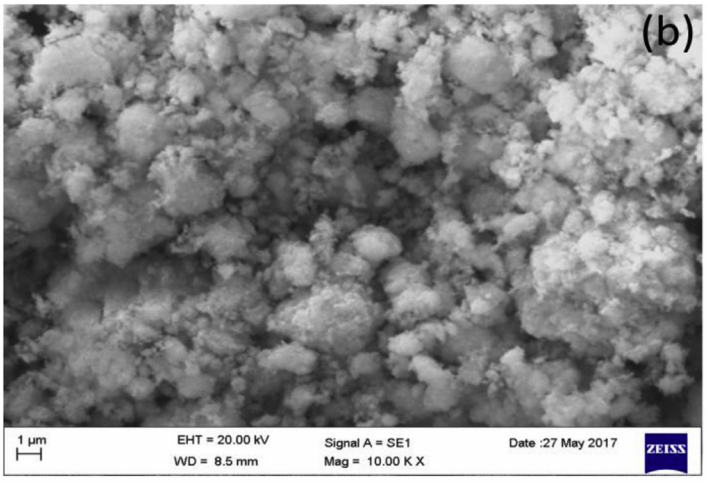
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WD = 8.5 mm
Signal A = SE1
Mag = 10.00 K X
Date :27 May 2017
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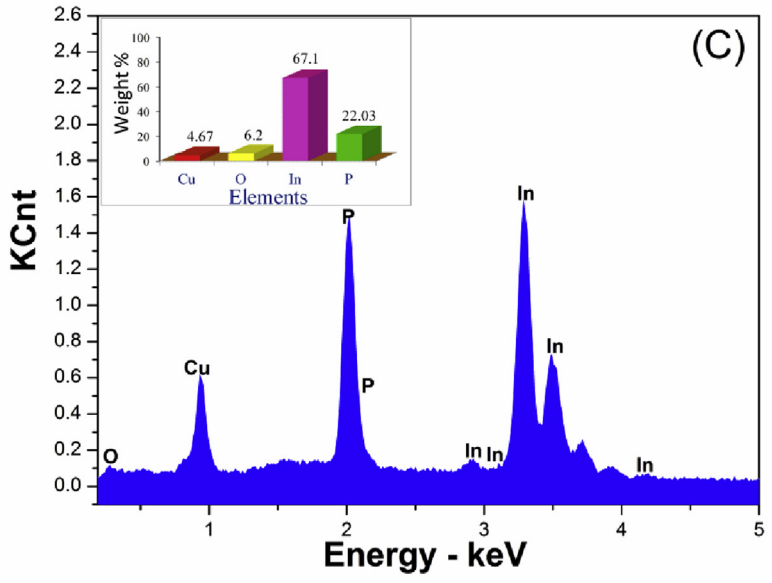
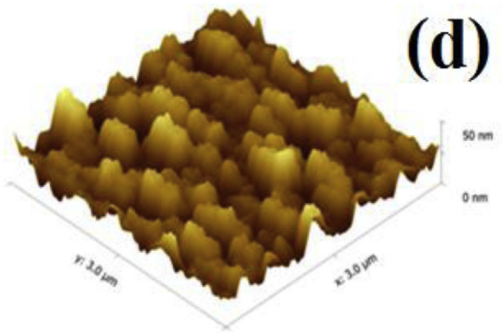

(C)
KCnt
Energy - keV
Weight %
Elements
Cu
O
In
P
4.67
6.2
67.1
22.03
O
Cu
P
P
In
In In
In
In


(d)
50 nm
0 nm