Precision Engineering 37 (2013) 897–901

Contents lists available at SciVerse ScienceDirect

Precision Engineering

journal homepage: www.elsevier.com/locate/precision

Monolithically integrated MEMS mirror array with low electrical interference in wavelength-selective switches

Tomomi Sakata[a,*], Fumihiro Sassa[a], Mitsuo Usui[a], Junichi Kodate[a], Hiromu Ishii[a,1], Katsuyuki Machida[b], Yoshito Jin[a]

[a] *NTT Microsystem Integration Laboratories, NTT Corporation, 3-1 Morinosato Wakamiya, Atsugi, Kanagawa 243-0198, Japan*
[b] *NTT Advanced Technology Corporation, 3-1 Morinosato Wakamiya, Atsugi, Kanagawa 243-0124, Japan*

ARTICLE INFO

Article history:
Received 26 November 2012
Received in revised form 26 April 2013
Accepted 10 May 2013
Available online 15 June 2013

Keywords:
Monolithic
MEMS
Electrical interference
WSS

ABSTRACT

This paper describes the fabrication of a microelectromechanical-system (MEMS) mirror array for a wavelength-selective switch (WSS). The MEMS mirror array, in which a lot of closely spaced adjacent mirrors are electrostatically operated, consists of a MEMS mirrors and a mirror-drive electrodes. In order to reduce electrical interference, comb-shaped ground walls with a high aspect ratio of about 20 are monolithically integrated with the MEMS mirror chip. Further, U-shaped gold electroplating walls are formed in the mirror-drive electrode chip. With these walls, each MEMS mirror successfully operates with low electrical interference.

1. Introduction

A wavelength-selective switch (WSS) will be a key component of a node of a reconfigurable optical add/drop multiplexer (ROADM) in the next generation of all-optical networks [1,2]. In a ROADM network, the WSSs can add and drop optical signals or let them pass through without converting them to electrical signals. Among the various types of WSSs, one of the most promising is a microelectromechanical-system (MEMS) mirror array module used in combination with free-space optics (Fig. 1), because it provides good characteristics, such as low insertion loss, low polarization-dependent loss, large bandwidth, and low power consumption [3–11]. For a MEMS mirror array module with a high fill-factor or narrower frequency grid, in which a lot of closely spaced adjacent mirrors are electrostatically operated, the problem is how to suppress the electrical interference that causes undesired operation of adjacent channels. For the practical use of WSSs, it is important to make the electrical interference as small as possible. To solve the problem of electrical interference, the novel MEMS mirror array (called the "hybrid array") shown in Fig. 2(a) has been proposed [12,13]. The MEMS mirror array consists of three parts: a U-shaped electrode chip, a MEMS mirror chip, and a pair of electrical-shield cap chips. Each mirror is suspended from two torsion springs and two cantilevers. Underneath each cantilever is a drive electrode that controls its movement. Therefore, for each wavelength channel, there are one mirror, two torsion springs, two cantilevers, and two drive electrodes.

When a voltage is applied to one of the U-shaped electrodes, the resulting electrical force pulls the cantilever above it downward, which produces a height difference between the two torsion springs coupled to the two cantilevers [12–14]. As a result, the mirror rotates. That is, the MEMS mirrors feature indirect drive coupled to the movement of the cantilevers. In such an array, the electric field generated between a mirror and its drive-electrodes is isolated by the conductive walls of the U-shaped electrodes and by the V-grooves of the conductive electrical-shield caps. Consequently, it does not affect the operation of adjacent mirrors at the level where the system requirement is satisfied [12,13].

The fabrication of a hybrid-array module involves flip-chip bonding the mirror chip to the drive electrode chip and then attaching the two electrical-shield cap chips. To realize such a hybrid array, the V-grooves of the shield caps have to be precisely placed above and between cantilevers to keep the cantilevers from coming into contact with the U-shaped electrodes. To avoid this horizontal and vertical alignment difficulty in jisso, which lowers yield, it is preferable to form the electrical-shield structures (such as shield structures) on the mirror chip simultaneously during the mirror fabrication processes.

* Corresponding author. Tel.: +81 46 240 2069; fax: +81 46 270 2322.
E-mail addresses: sakata.tomomi@lab.ntt.co.jp, sakata.tomom@aqua.plala.or.jp (T. Sakata).
[1] Present address: Toyohashi University of Technology, 1-1 Hibarigaoka, Tempaku-cho, Toyohashi, Aichi 441-8580, Japan.

0141-6359/$ – see front matter
http://dx.doi.org/10.1016/j.precisioneng.2013.05.008

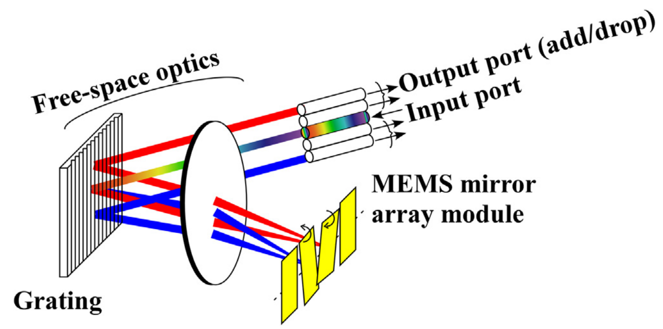

Fig. 1. Schematic of a 1 × N WSS, which consists of a MEMS mirror array module and free-space optics.

This paper describes a monolithic integration of a low-electrical-interference mirror in a MEMS mirror array for WSSs (called the "monolithic array") as shown in Fig. 2(b). For electrical isolation, the mirrors have comb-shaped ground (GND) walls instead of shield caps as an electrical-shield structure. The effectiveness of the walls in suppressing electrical interference between adjacent channels in the array is confirmed.

2. Design of comb-shaped walls

This section describes the design of the comb-shaped ground walls, which can be monolithically fabricated in a mirror chip, instead of shield caps having V-grooves, which are fabricated by silicon wet anisotropic etching with potassium hydroxide aqueous solution. The biggest structural difference between them from the viewpoint of electrical interference is the presence or absence of the conductive ceilings above the actuator of the cantilevers; that is, the cantilevers are encapsulated or not encapsulated with conductive material. In the case of the comb-shaped ground walls, which do not have the ceilings, the height of the comb-shaped ground walls becomes the most important factor in shielding the adjacent channels from the electrical field distribution from the adjacent channels. The required height of the comb-shaped ground walls, where electrical interference between adjacent channels will become negligible, was simulated by electromagnetic field analysis using the finite element method program ANSYS^{TM}. The simulation model was meshed with 2D 8-node electrostatic solid elements (PLANE 121). The simulation was carried out in three-channel mirror array, with channels 1 and 3 in the on-state (a maximum driving voltage of 200 V) and channel 2 in the off-state (0 V). Fig. 3 shows that the electrical potential distribution for ground walls with (a) 10-μm and (b) 100-μm thickness. In Fig. 4, the *x*-axis is the height of the comb-shaped ground walls, and the y-axis is the electrical field intensity in the center cantilever of channel 2 (see black cross marks in Fig. 3(a) and (b)). Fig. 4 shows that the electrical field intensity is almost zero for walls higher than around 100 μm, meaning that the electrical interference will become negligible (i.e. the same level as the effect of shield caps) with comb-shaped ground walls of such height.

3. Fabrication of MEMS mirror array and U-shaped electrode chips

The process for making a 50-channel mirror chip with the comb-shaped walls over the cantilever is shown in Fig. 5. It begins with a 6-in. silicon-on-insulator (SOI) wafer (Fig. 5(a)). The superficial silicon (Si) (resistivity of 1–3 Ωcm) is 5-μm thick, the buried oxide (BOX) is 1-μm thick, and handle Si layer (resistivity of 1–30 Ωcm) is 394-μm thick. First, mirror, torsion spring, and cantilever patterns are formed on the BOX by photolithography and a Bosch process with inductively coupled plasma reactive ion etching

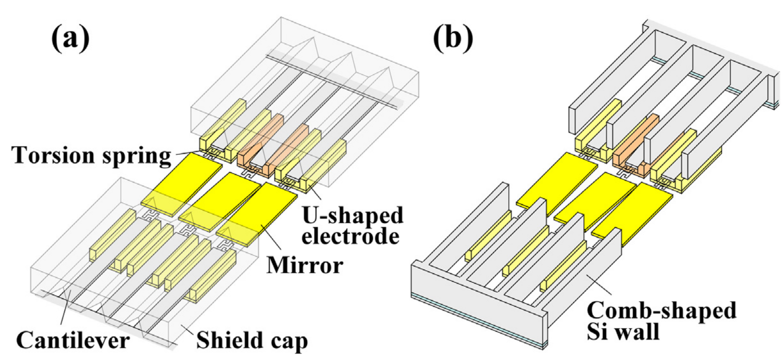

Fig. 2. Schematic of a MEMS mirror array module with (a) hybrid and (b) monolithic MEMS mirror arrays for WSSs.

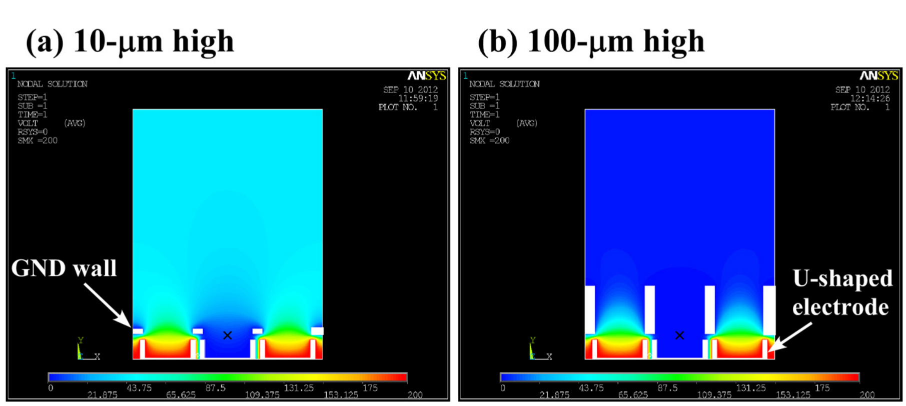

Fig. 3. Electrical potential distribution for ground walls with heights of (a) 10 μm and (b) 100 μm.