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Availability and reliability modeling of multicore controlled UPS for datacenter applications

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ABSTRACT

Modern data centers have to rely on continuous power to provide reliable and trustable services to their end users. Such power which comes from the main energy provider is most of the times supported by local uninterruptable power supply devices (UPS) which should therefore have a higher order of magnitude in terms of exploitability and reliability with respect to the hardware they are locally supporting. The reliability and availability performance of such systems must be therefore analyzed on both perspectives; the first one centered on the end user possibility to rely on a device every time it is needed and the second one aiming at a constant product performance improvement. These two different viewpoints can be far enough to lead to different product development strategies. In this manuscript a high efficiency modular UPS based on multicore control system for datacenter applications is presented and its reliability and availability figures discussed both from the designer and end user standpoints, under different operating conditions.

1. Introduction

The design of datacenter has recently pushed the research community towards the possibility to develop new models and design of uninterruptible power supply (UPS) systems able to grant high availability and reliability standards. Moreover, efficiency and regulation performance should be embedded at the state of the art designs in order to be competitive on the market proving in this way an additional constraint. Recently some authors [1–3] tried to analyze the reliability and availability of standard double conversion UPSs exploiting single processor for regulation and failure management. In particular such architectures based on single processor are of easy implementation but may be lacking, in case of control board failure, of an opportune redundancy degree [4–6] jeopardizing therefore the possibility to provide a predefined minimum availability threshold.

Additionally power efficiency requirement of datacenter applications may be hardly matched by single processor structures depending on the power size of the UPS. Some authors focused also the attention in the determination of the best suitable reliability and availability model applicable for general UPS devices [1–3] with the aim of strengthening their design. Most of the failures usually take place in the power section due to the high power requirements and currents involved (for 100 kVA up to 2MVA structures). Nevertheless it has been shown that depending on the design of the control section temperature gradients play crucial roles in determining the failure rate increase in the control section too [7]. The power supply board in particular of UPS, demanded to the generation of the power supply voltages for all the different sections of the control board, is heavily affected by power requirements and temperature gradients.

The concept of modular and multicore devices has been therefore recently introduced [8–9] with the aim of supplying more flexibility, and once proper consideration has been made on the system architecture, to provide overall higher system availability. Introducing system modularity actually allows for possible dynamic configurability in case of additional sudden power requirements or module failure, while allowing at the same time for performing maintenance activities having the system still online. Of course, modularity means higher costs because even if there can in principle be load sharing among all the installed modules, whenever maintenance is scheduled or needed, the single module of interest must be taken off the line.

Additionally, to implement a UPS modular structure requires the spread of the control logic boards across different sub-systems, in particular between the ones dedicated to the management of the power units only and the ones that have to be placed in

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parallel to provide the power needed for the specific application. In this work the author has considered a three phase structure divided into two main modules.

The first one, devoted to the control and management only and a second one, of a well-defined power, responsible for power generation. The modularity is given by the fact that whenever additional power is required it is sufficient to add in parallel to the previously defined basic structure other power modules connected in parallel according to the end user needs.

The present paper is arranged as follows: in Section 1 the introduction is provided with the aim of letting the reader become familiar with the outstanding problems. Section 2 is provided to describe an example of multicore modular system and to describe its main operating principles. In Section 3 some reliability and availability modeling considerations are provided on the basis of application assumptions [10–13]. Traditional reliability decomposition is performed in order to identify the critical block and availability analysis is performed based on the merging of database and field retrofit [14–15]. Finally in Section 4 simulation results are presented and in Section 5 the conclusions are summarized.

2. System description

The proposed basic architecture is a modular three phase UPS composed by a main logic controller structure named Input Output Bypass Module (IOBM) and a Base Power Module (BPM). The specific project relies on design from Borri even if the proposed simplified schematics apply to generalized structures. A simplified schematic of a sample UPS composed by a single IOBM and multiple BPM is represented in Fig. 1. The number of connected BPM units may vary depending on the desired output power from a single module up to 8 modules. Each BPM control unit is connected to the IOBM one through a communication/control bus, whereas the power line of the battery pack (centralized structure) embedded in the IOBM is connected both to the input–output three phase lines and to each single BPM as can be also seen in Figs. 2 and 3. The main control board CB of the IOMB module is devoted to keep the communication, control and management of the other equivalent CB boards present on each BPM module. This latter board (CB) on both the IOBM as well as on each BPM is divided into three separate sections equipped each one with a single core processor in order to: accomplish the AC/DC management for voltage (current) conversion, control and manage the inverter generation phase and activate the closing and opening of the output and battery static switches if needed, respectively. This is the main difference with respect to standard UPS designs where a single processor is demanded in managing all these functions on the same framework. In Section 3 such sections have been named as CB_Inv, CB_ACDC and CB_Static for convenience.

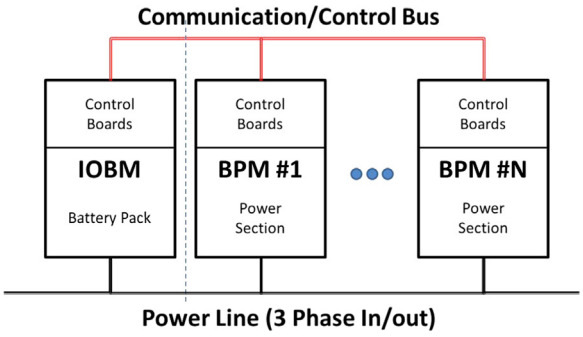

Fig. 1. Basic simplified structure of the modular UPS structure.

In Fig. 2 there is a detailed representation of the main components and boards of the IOBM module. The main components of this structure have been separated into logic boards (below the dashed lines of Fig. 2) and power sections (above the dashed line) to supply the battery pack in the centralized single battery configuration. From the input line (three phase Line In) through an electromagnetic filter (EMI FILTER) it is possible to supply the main section of the BPM module. From the BPM module the charge to the centralized battery is supplied and managed by the IOBM through a dedicated power switch up to the output line (three phase Line out) providing the power to the end user from the BPM module with the possibility to manage the output power switch and change to the bypass condition (from the main utility feeder) in case of need. All the local power management sections can be controlled by means of a series of electronic boards which are represented in Fig. 2 under the double dashed line.

As already mentioned, it has to be pointed out that the main control board CB is represented and arranged for this study with three main sections. The first one (CB_ACDC) is devoted to the control of the conversion step from AC/DC battery charger, then there is a section (CB_Inv) driving the inverter of the BPM in order to get the desired output waveform both in terms of amplitude, frequency and spectral characteristics according to the end user requirements. Finally the last section (CB_Static) is demanded in controlling the possibility to move from a condition where the power is supplied by the main utility feeder to the operating mode implying the UPS exploitation for power supply and vice versa. Moreover this section of the control board can be used to drive the connection of the battery pack to the BPM units. Direct control on the performance of the control board CB is accomplished through the A2 measurement section. Finally several manual switches (MBCB) are represented to take into account devices that are used in case some specific service operations have to be undertaken on the structure.

It is important to note that such division is possible thanks to the fact that this single board is equipped with three separated microcontrollers able to perform such operations independently from each other even in case of failure of one of the considered sections. Other accessory boards close the simplified description as the parallel module board I/O Par C1 devoted to communication with all the BMPs connected to the main IOBM, the power supply board and the measurement interface one (A2).

In Fig. 3 the representation of the basic three phase power module (BPM) is presented, which can be assembled together with an IOBM structure to generate the basic UPS structure.

The power section comprises the rectifier (PFC Rect), the IGBT bridge to convert battery DC voltage to line AC (Inverter) and a final line power switch (Static sw Inverter). The control section is similar to the one described in the IOBM structure because the two control sections of the modules have to be able to communicate in order to share information on feedbacks of the generated currents and voltages. Additional small boards for waveform filtering, notching and conditioning are presented (such as EMI FILTER, F1, A5, A6, A7, INT TL and INT PS A3) and embedded in this study even if their contribution to the overall system availability and reliability is not crucial. The two boards C2 and C1 are the communication and interface boards from and to the BMP modules and the IOBM one respectively.

A power supply unit for the control section is present finally as Power Supply A4 board on all the units of the UPS.

The proposed modular configuration has four main operating modes: the double high efficiency (OnLine) mode, the active filtering (CA) mode, the ECO mode and the ultra-high efficiency (UHE) one. All these operating modes allow the system for reaching efficiencies in the range 96% up to 99%. Of course, these operating modes can be managed by the main control board