Renewable and Sustainable Energy Reviews 89 (2018) 194–203

Contents lists available at ScienceDirect

Renewable and Sustainable Energy Reviews

journal homepage: www.elsevier.com/locate/rser

A review on carbon nanotube field effect transistors (CNTFETs) for ultra-low power applications

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ARTICLE INFO

Keywords:
MOSFET scaling
CNTFET
Device modeling
Simulation
Device fabrication

ABSTRACT

Presently, the battery life and high spectral efficiency are found to be a perennial problem in smartphones. With the advancement in the technologies towards 5 G, it has become mandatory to meet these challenges before problems are aggravated. Besides, CNTFET technology is found to be a promising field of research that is recommended in this review to solve these problems. The intention of this study is to provide an overview of most recent research on the state-of-the-art of CNTFETs. Several papers were reviewed that include the device modeling, simulation, device fabrication and its applications. However, the majority of these papers were observed to deal with digital applications, while the papers related to analog applications were limited. Moreover, this review provides the information regarding the results obtained from the device circuit performance and the scope for future prospects.

1. Introduction

Recent studies indicate that the supply of affordable and sustainable energy is required to maintain and improve the quality of life. Also, the sustainable energy influences technologies involving solar energy, hydroelectricity, wave power, wind energy, bioenergy, geothermal energy, and tidal power. Amongst these, the sun is a natural source of power and is expected to provide radiation for about 4 billion years. Thus, solar power (photovoltaic) systems are considered as a sustainable method to convert the energy from the sun into electricity [1]. The existing solar technology was found to limit efficiency and is acknowledged as a significant obstacle in implementing the large-scale generation of solar powered energy. Presently, photovoltaic (PV) panels were observed to convert only 16% of the sunlight that penetrates through them. Researchers at the Energy Department's National Renewable Energy Laboratory (NREL) have found out that Single-Walled Carbon Nano Tube (SWCNT) semiconductors could be favorable for photovoltaic systems because it can efficiently convert sunlight into electricity without losing much energy. Besides, the films made of SWCNTs were observed to have a large effective area conferring them high optical absorption and were found to contribute towards the energy harvesting utilizing Si. In this research, it was observed that up to 12% photo conversion efficiency was reported on employing photovoltaic devices and 100% of internal quantum efficiency (IQE) was reported [2].

In this review, it is noticed that majority of the PV devices need the electrons and holes present in the interface to be separated as soon as the absorption of the photons is processed and in return produces the electric current. During this process, the molecules involved will undergo a structural reorganization of the bonds resulting in energy loss and is referred to as reorganization of energy. Most recently, the NREL researchers have found that only little amount of energy is lost when the Single-Walled Carbon Nano Tube (SWCNT) semiconductors are combined with the fullerene molecules [3]. Therefore, this has opened new avenues in the research of Carbon Nanotube-based semiconductor device technology. A semiconductor is a significant part of the electronics industry, and entirely the computerized systems depend on them, including solar cells. A carbon nanotube field-effect transistor (CNTFET) corresponds to a FET that uses single or multiple carbon nanotubes as the channel instead of using bulk silicon as in the traditional MOSFET structure.

1.1. Scaling of MOSFET

In 1965, Dr Gordon E. Moore predicted an increase in the number of transistors integrated on an IC and suggested that it would be doubled every year [4]. This was presented as an observation in the initial phase. However, it became the base for the current semiconductor technology and paved a glorious path for more than 50 years of miniaturization and continues till date. Tragically, the recent prediction of

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https://doi.org/10.1016/j.rser.2018.03.021
Received 30 August 2016; Received in revised form 10 March 2018; Accepted 14 March 2018

the 2015 International Technology Roadmap for Semiconductors [5] states that the transistor could stop shrinking in another five years. This has been interpreted as death knell regarding Moore's Law. This is because the industry is not able to sustain the scaling of CMOS. The Si-MOSFET scaling has already moved towards its limiting value for several reasons including very high leakage currents, high power density, large parametric variations and decreased gate control which makes it less suitable for the near future ultra-low-power and ultra-high-speed applications. These drawbacks of the current technology lead to the investigations of various alternatives to keep the Moore's Law "get going". Furthermore, compared to conventional silicon MOSFETs, Carbon nanotube MOSFETs were found to provide better scalability and performance with suppressed short-channel effects and higher carrier mobility. This indicates future scope in the use of carbon as a promising candidate to replace silicon as the fundamental building material of integrated circuits in the future [6].

1.2. Investigation of various alternatives

Recent study, suggests the beginning of a new era with the advancement of technology beyond CMOS [7]. Many alternatives for MOSFET such as FinFET [10], TFET [11] and JLITFET [12] were proposed. However, those alternatives were not able to compete with CNTFET for numerous remarkable reasons. For many researchers, the quest for an ideal semiconductor to be used in FETs was quenched when Carbon Nanotubes (CNTs) were first shown to yield promising properties of these devices [7]. Its natural ultrathin body, efficient electron and hole transport properties and reasonable energy gap offer best solutions when compared to other semiconductors that are scaled to the sub-10 nm regime.

Therefore, it has been suggested and accepted by practically all the researchers and industry experts that CNTFET would be the device of choice for next generation VLSI chips with its high performance and smaller dimensions. This has also been emphasized by M. Schröter et al. [8] in the review article. Owing to the similarity between CNTFET and CMOS in case of operation principle and the device structure, the established CMOS design infrastructure can be performed in the CNTFET technology at ease. Also, the CNTFET based circuits are expected to be 3× faster than silicon transistors, while consuming the same power. Besides, Marani et al. stated that future scope of CNTFET will involve the investigation of the circuit model and its characteristics that could be used to provide the required power and could be tested on real-time devices [9].

The present review gives a rapid overview of important literature presented on carbon nanotube FETs for ultra-low power applications. Firstly, it reviews the technology involved in the fabrication of CNTFETs. Secondly, the reports on the Device Modeling of CNTFETs are compiled. Thirdly, the different design approaches and the simulated characteristics of CNTFETs are discussed. Finally, the possible applications of CNTFETs presented in the literature are compiled.

2. Process technology

The Process Technology refers to the overall integration process including lithography, doping, etching, deposition, testing methodology and the equipment used for testing etc. The front-runners in the process technology of CNTFETs are illustrated in this section.

2.1. CVD growth

CVD stands for Chemical Vapour Deposition. This process refers to the deposition of a material from a gas onto a substrate that involves chemical reactions. Chemical Vapour Deposition was utilized to determine the characterization of the films that will affect the morphology and crystallinity of the films. This study used appropriate deposition conditions to allow the coatings with superior photocatalytic activity to be prepared in a selected material [13].

Lorraine Rispal et al. [14] have reported on the fabrication of CNTFETs by using CVD (Chemical Vapour Deposition) Method. The work is summarized as below.

(1) In the first step, highly doped p-type silicon wafers were used to serve as back-gate.
(2) Oxidation was performed. Nickel (1 nm) on Aluminum (10 nm) was chosen to be the catalyst layer and was evaporated to facilitate SWNT growth.
(3) The next step involved annealing in inert ambient followed by CVD. Nitrogen followed by methane was supplied, and the CNT growth takes place for 10 mins.
(4) Finally, using lift-off method palladium source and drain electrodes were structured.

2.2. Improved CCVD method

The expansion of CCVD is Catalyst Chemical Vapour Deposition. This method is the enhanced method of CVD growth. In this method, metal catalysts are used for depositing materials on thermally sensitive substrates at low temperature. Therefore, the researchers suggest that the growth window of ACCVD will provide the platform to improve the robustness of ACCVD and the controllability over the product, thereby providing a better understanding of the growth mechanisms involved in Carbon Nano Tubes [15]. Martin Keyn and UdoSchwalke [16] conducted the experimental investigation of CCVD (Catalytic Chemical Vapour Deposition) grown CNTs. The highlights of the fabrication methodology are presented as follows.

(1) One-sided polished and p-doped silicon wafers were taken as substrates.
(2) Oxidation was carried out at 1000 oC in a dry oxygen atmosphere and the resulting oxide served as a gate oxide.
(3) The catalytic double layer is composed of a 5 nm aluminum layer and the 0.9 nm nickel layer. Annealing and CCVD were carried out successfully for 5 min
(4) Lift-off lithography was performed to realize the electrical contacts which are connected by the beforehand grown CNTs. The adhesion of the contacts was improved by annealing at 400 oC in forming the gas. Finally, undiluted HCl was used to remove the backside oxide.

Above approaches were able to supersede the previous processes by focusing on three parameters that made the difference which are (1) Oxygen plasma treatment (2) CCVD processing time and (3) Composition of the catalytic double layer. Such process of fabrication technique had big advantages when compared to other existing technologies. As a result of growing CNTs in-situ, all the undesirable effects of misplacement and possible damages were avoided. In this manner, CNTFET of excellent quality were produced.

2.3. Dielectrophoresis (DEP)

Dielectrophoresis is defined as the phenomenon in which a force is exerted onto a dielectric material when it is under the influence of a non-uniform electric field. The application of DEP-assisted integration approach was investigated on the sensor resistance distribution which has the ability to control the property of sensor distribution [17]. Furthermore, Zhigang Xiao et al. [18] have fabricated the CNTFET with dielectrophoresis method. The designed CNTFET has 3 μm as channel length and 10 μm as width. The step by step procedure is presented here.

(1) The silicon wafer of 350 μm thickness was taken as the substrate and it was oxidized for 20 mins at 1100o C temperature in the presence of moisture.