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Emerging challenges and materials for thermal management of electronics

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The rapid development of faster, cheaper, and more powerful computing has led to some of the most important technological and societal advances in modern history. However, the physical means associated with enhancing computing capabilities at the device and die levels have also created a very challenging set of circumstances for keeping electronic devices cool, a critical factor in determining their speed, efficiency, and reliability. With advances in nanoelectronics and the emergence of new application areas such as three-dimensional chip stack architectures and flexible electronics, now more than ever there are both needs and opportunities for novel materials to help address some of these pressing thermal management challenges. In this paper a number of cubic crystals, two-dimensional layered materials, nanostructure networks and composites, molecular layers and surface functionalization, and aligned polymer structures are examined for potential applications as heat spreading layers and substrates, thermal interface materials, and underfill materials in future-generation electronics.

Introduction

Over the past half-century, the drive for faster, cheaper computing and its long-associated requirements of increasing device density and progressive device miniaturization have served to push scientists and engineers to continually develop new and ever-improving materials, tools, processes, and design methodologies. As a result, electronic devices and their applications have been among the fastest advancing fields, with the characteristic dimensions of devices shrinking past the microscale and into the nanoscale within the matter of just two decades [1,2]. Today, many modern electronic devices operate with critical dimensions in the tens of nanometers. Moreover, minimum feature sizes of 14 nm and below are being targeted for next-generation technology nodes [1,2]. At the same time, new approaches at the die and package integration levels such as many-core architectures and three-dimensional (3D) chip stacking [3,4] are emerging as potential means of increasing computing performance without relying on reduced feature scaling alone. In addition, the rise of mobile devices and touchscreen applications has driven new research and development efforts into devices and materials compatible with transparent and/or flexible substrate design requirements. However, these exciting technological advances and emerging applications are also creating thermal challenges that may serve to ultimately limit their effectiveness, scope of implementation, or overall feasibility.

It has been well documented that the shrinking size and escalating density of transistors and other integrated circuit devices over time has enhanced computing capabilities at the cost of increasing power dissipation across the device, die, and system levels [5–7]. The power required for high performance computing applications on some modern processor modules can reach 200–250 W or more [8], leading to heat loads approaching as much as 1 kW for the processors alone in a four-socket computing system. While the high magnitude of the power dissipation certainly has implications at the system and data center levels, the power density and its spatial distribution at the die level is also of concern and can have important reliability and thermal management implications. The power dissipation in modern chip architectures

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can be highly non-uniform across the die surface, with localized functional areas where the power density is a factor of five to ten higher than the die average [9–12]. These power-dense regions can produce 'hot spots' – regions where local temperatures are significantly higher than the die average temperature [6,10–13]. Die-level hot spot sizes may range anywhere from ~500 μm^2 up to ~5 mm^2. For electronics the overall reliability is determined by the hottest region on the die rather than the average die temperature. As a result, hot spots can often dictate the required higher-level packaging and thermal management solutions including material selections, heat sink and cold plate design, and required pumping power at the system and facility levels. Thus, the thermal state at the device and die levels can have a far-reaching influence all the way up to the data center cooling requirements and environmental impact. In addition, if the required cooling cannot be delivered to keep the hottest region of a die under its stated temperature threshold the performance may be throttled down to reduce power. This unwanted reduction in performance is viewed as a last resort to be avoided if at all possible. Hence, there is a great desire to have enhanced, efficient heat spreading capabilities at both the 'local' single transistor device level as well as at the 'global' die and packaging levels in order to minimize the severity and influence of these hot spots.

The effectiveness of a heat spreading material is directly related to its thermal conductivity. As shown in Fig. 1, the room temperature thermal conductivity of known bulk materials used in electronics applications spans from about 3450 W m^{-1} K^{-1} in isotopically purified diamond [14] to on the order of 0.2 W m^{-1} K^{-1} for polymers such as poly(methyl methacrylate) (PMMA) [15]. In solids, heat may be transported by atomic lattice vibrations, the energy quantum of which is known as a phonon, as well as by charge carriers such as electrons and holes. For insulators and semiconductors the thermal conductivity is dominated by the contribution from phonons, while in metals the electronic contribution greatly outweighs the lattice component. The lattice thermal conductivity, κ_L, can be obtained from

$$\kappa_L = \sum_{\lambda} C_{\lambda} v_{\lambda} l_{\lambda} \quad (1)$$

where C_λ is the volumetric specific heat contribution from a phonon mode, v_λ is the phonon group velocity component along the temperature gradient direction, and l_λ is the mean free path component along the temperature gradient direction of phonons due to scattering with other phonons, defects, and grain boundaries. The summation is over all phonon modes $\lambda = k$, i with wavevector k and polarization i. A similar expression can be used to calculate the thermal conductivity contribution from electrons that dominate the thermal conductivity in metals. When the film thickness, line or channel width, or grain size of thin-film and nanostructured materials in electronic devices is reduced to be comparable to or smaller than the intrinsic mean free path of the dominant heat carriers in the corresponding bulk materials, enhanced boundary scattering reduces the thermal conductivity to be significantly lower than the bulk value [16–18]. This thermal conductivity suppression becomes more pronounced as the characteristic dimension decreases, which in turn may exacerbate the formation and severity of hot spots in electronics with sufficiently small feature sizes. The reduction in thermal conductivity with decreasing characteristic dimension is evident for the silicon (Si) material data plotted in Fig. 2.

In addition to reductions in feature size, another important trend lies in the increasing number of interconnect layers [19] with

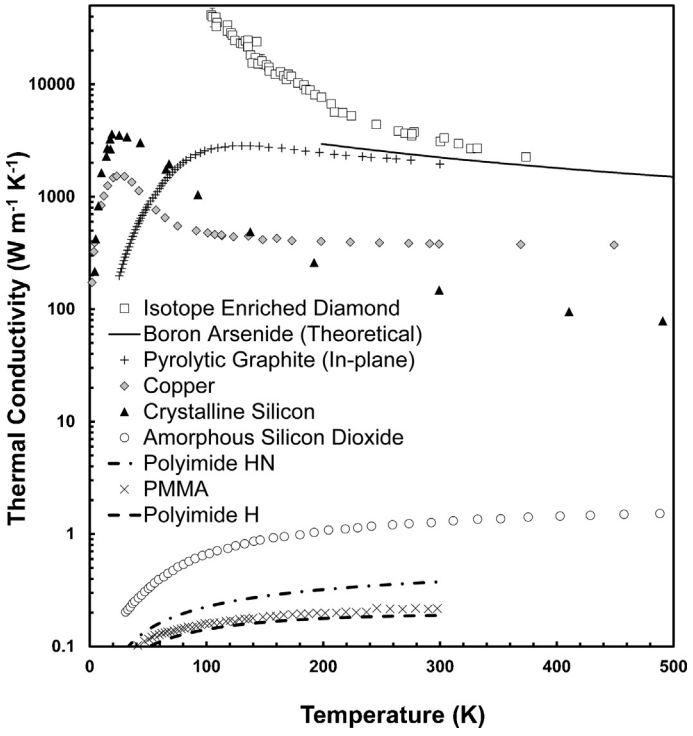

FIGURE 1

Representative temperature-dependent thermal conductivity values for various bulk solids: isotope-enriched diamond [14], boron arsenide [49], pyrolytic graphite [100], copper [101], crystalline silicon [46], amorphous silicon dioxide [199], poly(methyl methacrylate) (PMMA) [15], and two types of polyimide [200].

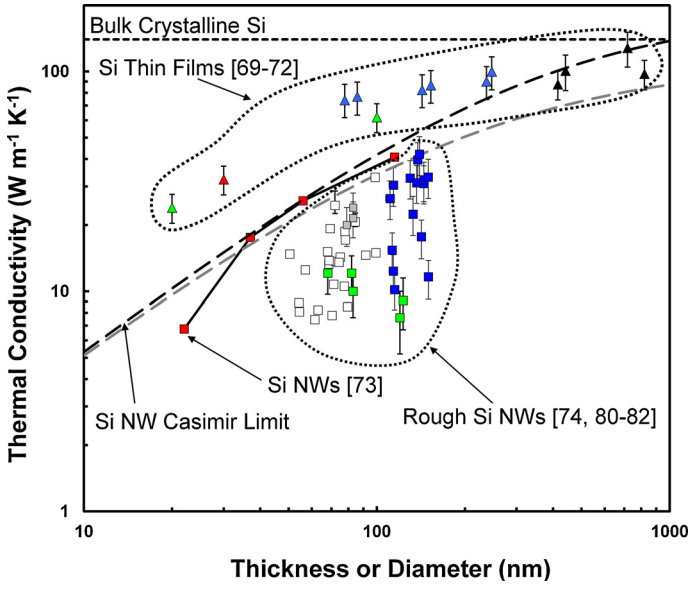

FIGURE 2

Room-temperature thermal conductivity of Si nanowires and thin films (in-plane) as a function of characteristic size compared to bulk values. The indicated black and gray dashed lines represent the Casimir limit for Si nanowires calculated for boron doping concentrations of 1×10^{13} and 1×10^{19} cm^{-3}, respectively [201].

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