Carbon nanotube electronics: recent advances

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Carbon nanotubes (CNTs) are quasi-one-dimensional materials with unique properties and are ideal materials for applications in electronic devices. Significant progress has been made on CNT electronics, and a doping-free approach has emerged from this research. This approach utilizes the contact control on the properties of field-effect transistors (FETs), preserving the perfect lattice of the CNT making it possible for CNT FETs to outperform state-of-the-art Si devices. Both *n*-type and *p*-type CNT FETs with near ballistic performance limits have been fabricated, symmetric CMOS devices have been demonstrated, and pass-transistor-logic, a circuit configuration that is more efficient than CMOS is being explored.

Introduction

While it has long been appreciated that semiconducting single-wall carbon nanotubes (CNTs) [1] have all the required electrical, thermal, mechanical and chemical properties [2] to be an ideal electronic material for next generation electronic devices [3–7], it has taken 15 years from the first reports on CNT field-effect transistors (FETs) [8–10] to the appearance of the first CNT computer [11,12]. The motivation behind the development of CNT electronics is the realization that the Si-based complementary metal–oxide–semiconductor (CMOS) technology will reach absolute limits on its performance by around 2020 [13], and improvements on transistor speed and performance will have to come from new materials rather than from scaling silicon further [14]. With the 2020 deadline in mind, researchers from both industry and academia started to actively work on emerging approaches. However, the choices are limited [15]. For a long time, the development of the semiconductor industry has been guided by the international technology roadmap for semiconductors (ITRS). In 2008, the ITRS committee realized the urgency and requested to its emerging research devices (ERD) and emerging research materials (ERM) working groups to determine which, if any, current approaches to providing a 'beyond CMOS' information processing technology are ready for more detailed road mapping and enhanced investment [13]. After careful evaluation of all potential emerging devices, including nano-electro mechanical switches, collective spin devices, spin torque transfer devices, atomic switches, single electron transistors, and carbon-based nanoelectronics, the ERD and ERM working groups recommended carbon-based nanoelectronics, including carbon nanotubes and graphene, for additional resources and detailed road mapping for ITRS as a promising technology targeting commercial demonstration in 5–10 years. The primary reasons for this recommendation are the extremely high carrier mobility in sp^2 carbon materials, that is CNT and graphene, and the possible application of the wrap-around gate geometry in CNT electronics [16–19] that provides the optimized electrostatic control on the channel current of FETs. Significant progress has also been made on other high mobility semiconductor based metal–oxide–semiconductor (MOS) FET technology, in particular InGaAs MOS FETs have been shown to be capable of scaling to the 10 nm node and below [20]. However, these recent developments have been made mainly on *n*-type FETs, and a logic InGaAs MOS FET technology for integration in a sub-10 nm CMOS node, in particular on a Si substrate still faces numerous challenges [20,21].

It is interesting to note that the FET is not the first transistor that was invented. The first transistor was a bipolar transistor, based on which the first integrated circuits were built. Initially MOS technology had hardly any advantages over bipolar, until CMOS came in, and nowadays more than 90% of the ICs are composed of CMOS FETs that are used in complementary and symmetrical pairs

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of *n*-type and *p*-type MOS FETs for logic functions. The two most important advantages of CMOS devices are high noise immunity and low static power supply. Significant power is only drawn from the power supply when CMOS devices are switching between on and off states, and consequently CMOS devices do not produce as much heat as other forms of logic, allowing a high density of logic functions on a chip [22].

A detailed comparison of CNT-based MOS FET technology *versus* other options, in particular Si nanowires, the best reported sub-10 nm Si-based transistors, and III–IV tunnel FET has been performed by IBM and Stanford scientists [23,24]. The CNT technology was shown to provide sizable improvements when scaled from an 8 nm to a 5 nm technology, while other alternatives provide virtually no power-performance advantage when scaled to these nodes. As illustrated in Fig. 1, CNT technology is predicted to be able to outperform silicon-based CMOS technologies by several technology generations and is the most promising CMOS technology that can be scaled down to 5 nm. Therefore, this review will be concerned mainly with the developments of high performance CNT CMOS FETs that outperform Si CMOS FETs. This approach uses high quality parallel arrays of CNTs grown directly on an insulator, such as SiO_2 or quartz, and no purification or other chemical treatments are made to these CNTs, and a doping-free process is used for the fabrication of CNT devices to preserve the perfect sp^2 lattice of the CNT [25].

While this review is not mainly concerned with the ultra-long CNT growth on an insulating surface, there exist several excellent reviews on this subject [26–30] and interested readers are referred to these reviews. Significant progresses have also been made on CNT electronics based on CNT thin films which are composed of mixed metallic and semiconducting CNTs [12,31–33]. Effects due to metallic CNTs are eliminated via chemical treatments such as purification, electric breakdown, or utilizing network type CNT configurations [34–38]. While this type of approach may be used in unusual electronics, such as flexible and stretchable electronics [39], and to build complex systems such as CNT radio [40], frequency doubler and mixers [41], and even a computer [12], the electric properties of the CNT are compromised by these processes. In addition, instead of using CMOS configuration, *p*-MOS that utilizes only *p*-type FETs is usually utilized which compromises the performance of the CNT circuits making it unsuitable for building high performance and low power logic systems that will ultimately outperform Si CMOS technology.

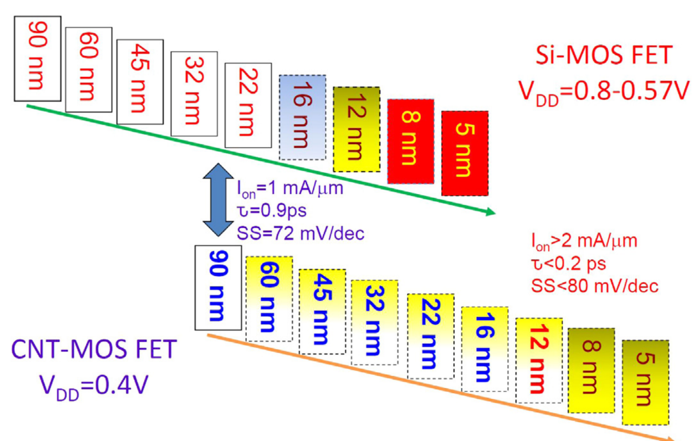

FIGURE 1

Comparison of Si and CNT MOS FET roadmaps down to 5 nm transistor technology.

Although graphene has extremely high carrier mobility, unlike semiconducting CNTs, graphene does not have an energy band gap. Without a band gap, it is not capable of serving as a digital switch. A small band gap can be opened when graphene is cut into a small ribbon, for example sub-5 nm wide, but carrier scattering at the edges increases making it inferior than a CNT. In principle graphene could provide excellent transistors for radio-frequency (RF) applications, but graphene devices lack the intrinsic device gain. Various methods have been proposed to overcome these challenges, and interested readers are referred to the excellent reviews [42,43].

Basics of FET

Integrated electronics has come a long way since the invention of the first transistor in 1947 and the fabrication of the first integrated circuit (IC) in 1958 [44]. However, the progress on Si-based ICs has mainly been achieved by simply scaling down an extremely important device, that is the FET, and any progress made on improving the efficiency of this device will have significant impact on the IC industry. A classic FET is a three terminal device which includes such key components as the source (S), drain (D) and gate (G) electrodes; a channel between the source and drain; and a dielectric (typically oxide) separating the gate from the channel (Fig. 2a).

The basic functions of a FET are to control the device resistance or drain–source current I_{DS} in the channel, mainly via the gate voltage V_G, and to amplify signals. As illustrated in Fig. 2b, the switching behavior of a FET is characterized by two key parameters. One is transconductance which reflects the magnifying ability of the FET, and the other is sub-threshold swing (SS) which measures how fast a FET can be switched from an off current or off-state to an on current or on-state. In general, the smaller the SS is, the faster the FET. For an ideal FET at room temperature, the theoretical value for SS is 60 mV/decade. While for long channel FETs, both planar and non-planar (Fin-gate) Si FETs have SS values between 60 and 80 mV/decade, suggesting excellent control on the channel current. However, the Si FET begins to lose its control on the channel current as the gate length is scaled down to sub-20 nm regime (Fig. 2c). A recent study using a local bottom gate geometry exhibit a superb SS of 94 mV/decade for a *p*-type CNT FET and a gate length of 9 nm [23], and a much lower SS of 74 mV/decade was obtained for an *n*-type CNT FET using a more efficient top-gate geometry with a gate length of about 15 nm [45]. This superior ability of the CNT FET on the channel resistance resulted from the unique band structure and the ultrathin body of the CNT, which is un-parallel for Si and other semiconductors based FETs, making the CNT CMOS FET the most promising device for technology node down to 5 nm.

History and basics of CNT FET

Schottky barrier CNT FET

The CNT FETs were first developed by Dekker's group at Delft university and by IBM for a convenient back-gate geometry [8,9]. While the device (Fig. 3a) is similar to the Si-based FET as shown in Fig. 2a [9], the detailed device physics are very different [46,47]. In Si or other conventional semiconductor based FETs, carriers are

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