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A novel readout integrated circuit with a dual-mode design for single- and dual-band infrared focal plane array

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HIGHLIGHTS

- A pixel readout circuit with the ability to choose different sensors is proposed.
- Conventional transimpedance amplifier layout area in pixel is reduced.
- The transimpedance amplifier satisfies the requirement of NPN and PNP sensors.

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ABSTRACT

This paper proposes the design of a dual-band readout circuit structure for infrared imaging systems. The design uses a capacitive transimpedance amplifier with a single-stage amplifier and a switch mode. It has the advantages of a simple structure and a small pixel area. Moreover, the switch mode provides the choice of different sensing modules. To verify the feasibility and applicability of the proposed design, a 10×8 experimental chip was designed and implemented using a TSMC 0.35 μm 2P4M CMOS 5 V process. The experimental result shows a sensing photocurrent from 10 pA to 10 nA of a forward bias detector signal. A reverse-bias detector photocurrent is 12 pA to 10 nA. Total chip power consumption is less than 9.1 mW within the output buffer. Power-per-pixel is 2.2 μW/pixel, and the pixel linearity is more than 99%. A description of the design and the latest experimental test results of this device are reported in this paper.

1. Introduction

Interest in using infrared (IR) imaging systems for military surveillance has been growing. They have recently been widely used in medical diagnostic instruments and applications of monitoring life signs in patients. In the IR image system architecture, there are lenses, IR focal plane arrays (IRFPAs), readout integration circuits (ROICs), signal-processing circuits, display circuits, and some form of cooling. The IR wavelength is in proportion to light intensity. IR sensors measure the physical change of received IR radiation, which is transformed into an electrical signal and delivered to the readout circuitry to display the change in IR signal. Different sensors, such as short-wavelength InGaA, mid-wavelength InSb, and long-wavelength HgCdTe, respond to different IR wavelengths, thus responding to different energy levels. To support these various sensors, it is important to have a readout circuitry design that is capable of supporting a multi-wavelength IR detector system.

The earliest literature about readout circuits for IR sensors was published approximately 30 years ago [1–9]. The technology developed from early source-follower-per-detector (SFD) [2,3] and direct injection (DI) [1–3] methods, to buffered direct injection (BDI) [2,6], capacitor transimpedance amplification (CTIA) [7,8], gate modulation input (GMI) [9,10], switched current integration (SCI) [11], and buffered gate modulation input (BGMI) [10,12,13]. DI, BDI, and CTIA are currently the three main readout circuit architectures in use [14–19].

DI is the earliest method used in photodetector ROIC architecture [1]. The DI input signal is applied to the source input of a transistor. The output of that transistor is integrated by a bank of integrating capacitors, and then applied to the gate of a source follower transistor. DI possesses the characteristics of a simple structure, low power, and small area. For these reasons, DI is suitable for mid-wavelength IR (MWIR) detectors such as quantum well IR photodetectors (QWIPs). However, DI has low injection efficiency when the input photocurrent is small. Injection efficiency can be improved by using BDI with improved injection efficiency and input impedance, making BDI suitable for use with long-wavelength infrared (LWIR) sensors [16,17]. However, the buffer amplifier, with greater charge storage capacity, increases power consumption and adds to unit cell complexity. CTIA has the advantages of a stable bias voltage, small input impedance, and low noise, so that

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it is suitable for short-wavelength infrared (SWIR) sensors with small input current. To increase the range of IR light detection, a design for a dual-band IR ROIC was recently developed [19,21–32]. In this ROIC, there are multiple possible combinations of bands, such as the mid/long-wavelength IR (M/LWIR) and short/mid-wavelength IR (S/MWIR). In addition, the design of readout circuits is based on the architecture of the sensors used. There are two main architectures: pixel-interlaced mode and pixel-mixed mode. To coordinate with M/LWIR pixel-interlaced sensors, the interlaced mode of readout circuits requires two frame periods when reading two signal frames. The readout circuit with the interlaced mode can be achieved by a modification of single-band readout circuits so that its design is simplified. The hybrid mode of readout circuits only needs one frame period when reading two signal frames. However, more output buffers are required, which increases power consumption. In summary, the use of CTIA, DI, and BDI structures is a popular trend; thus, readout circuit design selection is a basic priority [20,26–36].

This paper proposes the design of a dual-band readout circuit using a CTIA structure in pixel circuits for IR imaging systems. The system architecture of the ROIC is shown in Fig. 1a, and includes the digital control circuit and analog detecting circuit. In the digital control circuit, the FSYNC signal controls the integration time of pixels and the frame time. The LYSNC signal controls the selection time for each row, which includes the processing time of columns and other internal analog setting circuits. Column time is controlled by the main clock, and the output time of each pixel is controlled by the rate of output from the buffer stage. The speed of the readout circuit is determined by the frame time [37]. Digital timing is shown in Fig. 1b. CTIA is used in the pixel-detecting circuit of the analog detecting circuits. The column stage includes the skimming circuit and the output buffer.

Traditionally, CTIA depends on the amplifier. In CTIA, the negative feedback is using the capacitance component and the input terminal is using the resistance component to constitute the integrator circuit [12,14,16]. The photodetector can be regarded as a current source, which includes the resistance and a capacitor. Because of the structure of the negative feedback circuit, the impedance of the negative feedback is small at the current source so that the photocurrent source signal is small, corresponding with SWIR sensors such as InGaAs and InSb. CTIA requires a stable bias voltage of sensors, which can be adjusted by controlling the input positive terminal. The equivalent internal resistance and the capacitance of sensors affect the operating bandwidth of CTIA. Because of this characteristic of the sensors, the small sensing current leads to the long integration time. Therefore, the range of system applicability decreases when CTIA is used in sensors with a small equivalent internal resistance and capacitance. In general, CTIA used for small sensing signals needs to overcome the problem of its integration capacitor limited to the area, bandwidth, and power of the amplifier. In conclusion, because in recent years the sensors have become diversiform and multifunctional, and because the array size is larger, the area, power, and injection efficiency are challenges to overcome for CTIA.

Certain papers have presented the concept of a CTIA architecture using a single-stage CMOS amplifier to solve the area problem [12,14,16]. This design uses switches in the readout of dual bands, and applies reverse bias to the P–N–P photodetector and forward bias to N–P–N photodetectors. The primary reason for detector bias direction is to select different wavelengths [37–42]. The switch mode can provide the choice of different sensing modules. The single-stage CMOS amplifier has the advantages of a simple structure and a small pixel area. In addition, a 10×8 experimental chip has been designed and implemented using a TSMC 0.35 μm 2P4M CMOS process. The experimental result shows the feasibility and applicability of the proposed architecture.

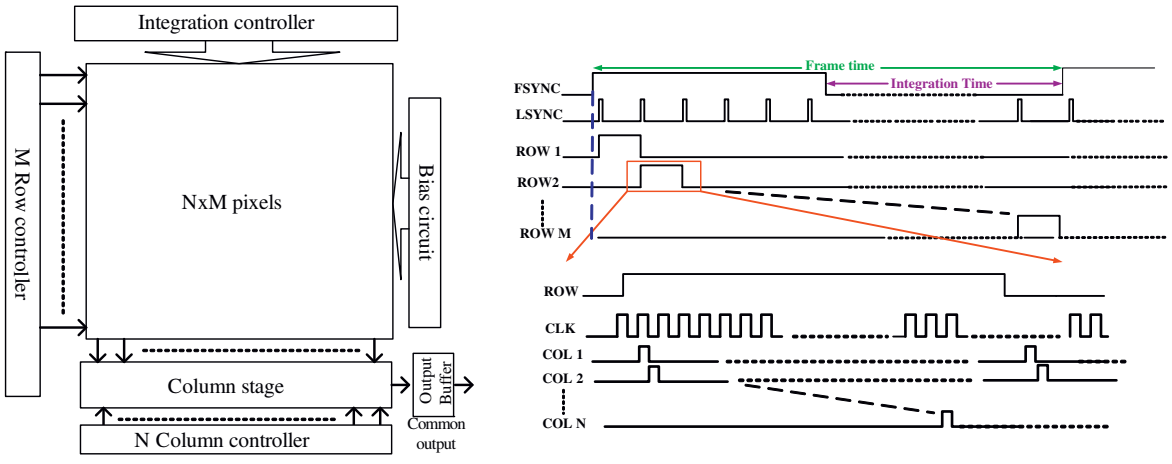
This paper is organized as follows. The first section details the background and illustration of ROIC, the second section interprets the architecture and design method of each sub-circuit, the third section describes the simulation and layout of the circuit, the fourth section illustrates the results of the circuit measurement, and the fifth section offers a summary and discussion.

2. Readout circuit design

This section presents an interpretation of the architecture and design method of sub-circuits, including an illustration of the pixel circuit and the skimming circuit.

2.1. Illustration of the pixel circuit

The architecture of the pixel circuit, which is a P–N–P sensor, is shown in Fig. 2. It uses Mcp1 as the gain amplifier stage, Mcn2 is the active load, and the overall gain is 40 db. The bias voltage of the sensor is adjusted by the VDETCOM source of Mcp1. The design and layout affect the threshold voltage V_T. The pixel readout circuit



(a) Diagram of the readout circuit system (b) Digital timing of the readout circuit

Fig. 1. The system architecture of readout circuit.