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Oxide reduced silicon nanowires

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ABSTRACT

Core crystalline silicon nanowires with a heavily reduced amorphous shell have been successfully synthesised using palladium as a metal catalyst. We present two approaches to reduce the oxidation of the nanowires during the thermal annealing growth. The ratios of the amorphous shell to crystalline core of the nanowires produced, from the two methods, are compared and show a remarkable drop (hence thinner oxide) compared to wires fabricated using currently available techniques. In addition, a focused ion beam was utilised to contact the oxide-reduced nanowires for transport measurements, without first removing the thin oxide shell. The oxygen-reduced core-shell silicon nanowires showed a very low electrical resistivity ($4 \times 10^{-1}\ \Omega$ cm). Our novel approach presents a new alternative to the production of low cost, high yield, highly conducting silicon nanowires offering a wide range of opportunities for semiconductor based technology.

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1. Introduction

One dimensional structured silicon nanowires (SiNWs) have an extensive appeal to a wide community owing to their outstanding electronic and optical properties. Different SiNWs synthesis methods have been reported, including – but not limited to – physical vapour deposition (PVD) [1,2], chemical etching [3] and thermal annealing [4–11]. In the chemical etching growth method, the SiNWs grow through a top down growth approach while with PVD as well as thermal annealing, these wires have been reported to grow through a bottom up approach which utilises vapour liquid solid (VLS), vapour solid solid (VSS) or solid liquid solid (SLS) growth mechanisms [12–14]. From the abovementioned synthesis methods with varying experimental conditions, a variety of nanowire configurations can be grown, such as crystalline silicon [15], amorphous silicon oxide nanowires [4–6], crystalline silicon oxide (SiO_x) nanowires [7,8], or crystalline core-amorphous shell silicon nanowires [9–11]. With these approaches, silicon-based nanowires are used in many different applications such as field effect transistors (FET) [16], biological and chemical sensors [17], and in solar energy conversion (e.g. solar hydrogen generation) [18].

The focus of this work is on SiNWs synthesised using thermal annealing and the produced wires characteristics. Such SiNWs grow via the SLS mechanism, which is an attractive method for producing SiNWs with long lengths (up to several hundreds of micrometres) in large quantities without using an external silicon source. Deepak et al. [7] synthesised crystalline SiO_x nanowires through the SLS mechanism and the nanowires were found to exhibit a uniform diameter of ~70 nm with a 30 nm crystalline core, hence a 1.33 amorphous to crystalline core (a-c) ratio. A mixture of fused silica and activated charcoal powder was used as a source material during the growth of the SiO_x nanowires. Other researchers [9–11,19,20] reported c-Si nanowires, also sheathed with a layer of a-SiO_x, using the SLS growth method. Cui et al. [11] highlighted the importance of the core-shell SiNW heterostructures for high capacity and high current battery electrode applications. These versatile nanowires have also been used as the building blocks in field effect transistors (FET). Cui et al. [16] found that the thermal annealing of the core-shell SiNWs increases the average transconductance. Lee et al. [20] synthesised nanowires

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using Ni as the catalyst and examined their electrical properties. They, however, had to first etch away the amorphous shell to expose the ~10 nm wide crystalline silicon core, followed by the fabrication of Ti/Au contacts, creating a silicon nanowire FET device.

In this work palladium (Pd) was used as a metal catalyst because it forms a liquid solution (metal silicide alloy/droplets) [21] on the surface of the silicon substrate at high temperatures (near the eutectic temperature) making it a good catalyst for the growth of SiNWs. In addition, palladium is a platinum group metal (PGM) and therefore is inert to chemical reaction. During palladium silicide droplet formation, the reaction between palladium and silicon at the Pd-Si interface at low temperatures results in the formation of Pd-silicide, with Pd_2Si reported to be the first and stable phase at low temperatures [22,23]. However, at high temperatures of around 850 °C, transformation to the second phase (PdSi monosilicide) does occur. According to the Pd-Si phase diagram [21], the PdSi phase is expected to transform from solid to liquid at about 892 °C (eutectic temperature) and no silicon rich phase forms above this point. Therefore, with the additional supply of silicon from the silicon substrate at high temperature, the droplets supersaturate with silicon and initiate the growth of the SiNWs.

2. Materials and method

For the growth of OR (oxide-reduced) SiNWs utilising the SLS growth mechanism, a molecular beam epitaxy (MBE) system (MECA 2000) was used to deposit a palladium catalyst onto a n-type silicon (100) substrate, 5 cm in diameter, 280 μm thick and with a resistivity of 1–10 ohm cm. Prior to the deposition, the silicon substrate was cleaned using a RCA cleaning procedure [24] followed by drying with N_2 gas. The clean and dry substrate was immediately transferred into the MBE chamber which was evacuated to a pressure of 8×10^{-9} mbar before starting the palladium deposition at 0.1 Å/s. The palladium-coated silicon wafer was cut into samples of approximately 1 cm × 1 cm. Some samples were further coated with carbon using an AJA magnetron sputter system at a pressure of 4×10^{-3} mbar, with the aim to reduce the oxidation [9] of the SiNWs during growth. The SiNWs were grown at 1000 °C using an STF 1200 series split tube furnace under a mixture of argon (300 millilitres/minute (ml/m)) and methane (10 ml/m) gas. Using the secondary electron mode of a Zeiss Auriga field emission scanning electron microscope (FEG SEM) operated at an accelerating voltage of 5 kV, micrographs of the annealed samples were acquired.

The structural properties of the SiNWs were then investigated using a high-resolution transmission electron microscope (HRTEM, FEI Tecnai G2 F20 X-Twin) operated at an accelerating voltage of 200 kV. For harvesting purposes, the SiNWs were first removed from the silicon substrate using a scalpel. A few drops of ethanol were placed on the silicon surface containing the nanowires, followed by gently scratching of the surface to obtain an ethanol solution with silicon nanowires. A copper grid, covered with an amorphous carbon thin film, was pulled through the ethanol-silicon nanowires solution. The grid was dried in air before transferring it into the HRTEM chamber for analysis.

3. Results

3.1. Silicon nanowire synthesis and characterization

The SEM micrograph in Fig. 1 (a) shows a wool-like SiNW structure rooted onto the substrate after annealing the palladium-coated silicon substrate at 1000 °C for 5 min in an argon atmosphere (300 ml/m).

The nanowires have an average diameter of 60 nm with lengths up to several tens of micrometres. In addition, palladium silicide tips, indicated by the red arrows in Fig. 1 (a), were observed. In Fig. 2 (a), a TEM micrograph shows a core-shell structure consisting of a crystalline silicon core sheathed with an amorphous SiO_x. Using image J software, the average thickness of the crystalline core and amorphous shell of these nanowires were found to be approximately $7.67\ \text{nm} \pm 0.17\ \text{nm}$ (~8 nm) and $31.16\ \text{nm} \pm 0.39\ \text{nm}$ (~31 nm) respectively, giving a total thickness of around 70 nm.

In an attempt to reduce the silicon nanowire oxidation (thick green layer in Fig. 2 (a)), carbon incorporation methods were employed. In the first approach, methane gas (mixed with argon gas) was introduced during the growth process. Fig. 2 (b) shows a TEM micrograph of a sample annealed in a mixture of argon (300 ml/m) and methane (10 ml/m). Although the entire wire was still sheathed with an amorphous oxide shell, this outer SiO_x shell layer was heavily supressed from around 30 nm to approximately 9 nm as shown in Fig. 2 (b). Furthermore, the crystalline core of these nanowires was found to have increased from about 8 nm to around 12 nm. Consequently, the overall SiNW diameter was reduced from 70 nm to about 30 nm. To further reduce the outer oxide shell, a second method of depositing an amorphous carbon coating onto the palladium-coated silicon substrate together with the introduction of the methane argon gas mixture was implemented. These SiNWs were synthesised at the same temperature and duration as the two previous growth runs. A TEM image of this sample is shown in Fig. 2 (c), a zoomed image of Fig. 1 (c), region 1. The TEM image, Fig. 2 (c), shows that the oxidation of the nanowire

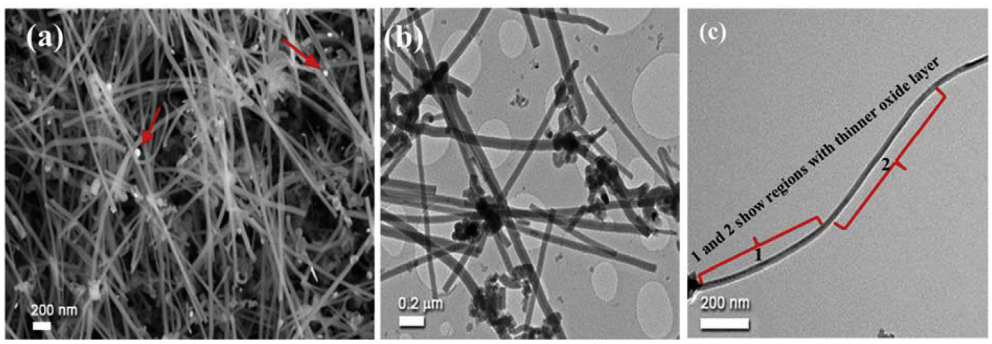

Fig. 1. (a) SEM showing wool-like silicon nanowires after annealing Pd-coated n-Si⟨100⟩ substrate at 1000 °C for 5 min, in Ar gas. Red arrows are pointing to the SiNWs tips. (b) TEM image of the silicon nanowires. (c) TEM image of a SiNW grown by first depositing an amorphous carbon coating onto the palladium-coated silicon substrate and then introducing a methane argon gas mix (method 2). The image shows the regions appears to be under stress hence thinner oxide layer growth occurred. (For interpretation of the references to colour in this figure legend, the reader is referred to the Web version of this article.)

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