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## Zero bias conductance peak in InAs nanowire coupled to superconducting electrodes



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#### ABSTRACT

We report the occurrence of the zero-bias conductance peak (ZBCP) in an InAs nanowire coupled to PbIn superconductors with varying temperature, bias voltage, and magnetic field. The ZBCP is suppressed with increasing temperature and bias voltage above the Thouless energy of the nanowire. Applying a magnetic field also diminishes the ZBCP when the resultant magnetic flux reaches the magnetic flux quantum h/2e. Our observations are consistent with theoretical expectations of reflectionless tunneling, in which the phase coherence between an electron and its Andreev-reflected hole induces the ZBCP as long as time-reversal symmetry is preserved.

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Nano-hybrid superconducting devices, which consist of lowdimensional nanostructures in contact with superconducting electrodes, provide a useful platform for developing novel quantum information devices. In particular, InAs nanowires (NWs) have attracted intense interests as a good material system for fabricating nano-hybrid superconducting devices owing to their outstanding electrical properties, such as high electron mobility, low effective mass, and relatively easy formation of low ohmic contacts. So far, a supercurrent transistor [1], NW quantum dot [2], quantum electron pump [3], Cooper pair splitter [4], and gate tunable superconducting qubit [5,6] have been developed with InAs NWs. As a signature of a Majorana fermion, which is a particle identical to its own antiparticle, the zero-bias conductance peak (ZBCP) has also been observed in an InAs NW coupled to a superconducting electrode [7]. Because the ZBCP can also be caused by reflectionless tunneling [8] due to an incomplete superconducting proximity effect, more extensive studies are required to verify the physical origin of the ZBCP observed in InAs NWs.

The superconducting proximity effect in nano-hybrid superconducting junctions can be understood with the Andreev reflection [9], where an electron incident upon the interface between a normal metal (N) and superconductor (S) can be retro-reflected into the N region as a phase-conjugated hole while leaving a Cooper pair in the S region. As a result, the Andreev reflection occurring at an ideal N-S interface results in a twofold increase of the conductance for bias voltages smaller than  $\Delta/e$ , where  $\Delta$  is the superconducting energy gap. With a non-ideal N-S interface, there exists a finite probability for the incident electron to be partially reflected as an electron and also retro-reflected as a hole via the Andreev reflection. When the mirror-reflected electron undergoes several scatterings with disorder centers in the N region and is incident on the N-S interface again, an additional Andreev reflection can occur. This results in another retro-reflected hole tracing back the previous scattering paths and continuing successive Andreev reflections. This process, which is called reflectionless tunneling [8], can also cause a ZBCP in a sample including the N-S interface. So far, the ZBCP due to reflectionless tunneling has been observed in several nano-hybrid superconducting junctions made of graphene [10] and InAs NW [11]. Though the characteristic voltage and temperature for the ZBCP are theoretically expected to be determined by the Thouless energy  $E_{Th}$  [8], the observed value of the characteristic voltage was much smaller than  $E_{Th}/e$  [11]. This discrepancy between theory and experiment has been attributed to a degradation effect at the N-S interface, resulting in a reduction of the diffusion constant and  $E_{\text{Th}}$  [11]. Here, we report the observation of a ZBCP obtained from an InAs NW in contact with

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superconducting PbIn electrodes. Our extensive studies of ZBCPs with a varying bias voltage, temperature, and magnetic field revealed that our observed ZBCP is due to the phase-coherent quantum electronic transport, which is consistent with the reflectionless tunneling theory.

InAs NWs were grown on a Si substrate by ultrahigh vacuum molecular beam epitaxy with gold particles (~50 nm diameter) as the catalyst [12]. The as-grown InAs NWs were transferred to a highly p-doped Si substrate covered by a 300 nm thick oxide layer. Source and drain electrodes were patterned by conventional ebeam lithography, followed by e-beam evaporation of 170 nm thick PbIn film. Prior to the metal deposition, the NW surface was cleaned with an Ar ion beam to remove a presumed native oxide layer. The PbIn alloy source was made by using a mixture of lead (Pb) and indium (In) pellets with a weight ratio of 9:1. The 10 nm thick Au film was used as a capping layer. Fig. 1a shows a scanning electron microscopy (SEM) image of sample D1 after the device fabrication process was completed. The superconducting transition temperature and perpendicular critical field of the PbIn film were obtained as  $T_C = 7.3 \text{ K}$  and  $B_C = 0.24 \text{ T}$ , respectively [13]. The differential conductance dI/dV was measured by using a standard lock-in technique of superimposing a small AC signal with a frequency of 37.77 Hz onto the DC bias current. For low-noise measurement, two-stage resistor-capacitor (RC) filters (cutoff frequency = 10 kHz) and  $\pi$  filters were connected in series to the measurement leads [14]. We note that all data in Figs. 2 and 3 were obtained from sample D1.

Fig. 1b displays the conductance G of sample  $\mathbf{D2}$  as a function of the backgate voltage  $V_{\rm g}$  at T=10 K. This indicates n-type conduction of the InAs NW. The small conductance oscillations superimposed on n-type behavior are attributed to universal conductance fluctuations associated with the phase-coherent diffusive motion of the conduction electrons along the InAs nanowire [1]. The electron mobility was  $\mu = \mathrm{d}G/\mathrm{d}V_{\rm g} \times L^2/C_{\rm g} = 3800~\mathrm{cm}^2/\mathrm{Vs}$ , where L is the channel length and  $C_{\rm g}$  is the gate capacitance between InAs NW and the Si substrate [15]. The diameter and channel length of sample  $\mathbf{D2}$  are  $d=60~\mathrm{nm}$  and  $L=590~\mathrm{nm}$ , respectively, while the carrier density is about  $n\sim2.8\times10^{17}~\mathrm{cm}^{-3}$  and the mean free path is  $l_{\rm m}=41~\mathrm{nm}$  at  $V_{\rm g}=0~\mathrm{V}$ . Dimensions for sample  $\mathbf{D2}$  are  $d=60~\mathrm{nm}$  and  $L=590~\mathrm{nm}$ , respectively.

When the temperature was lowered below  $T_C$ , the resistance of sample **D1** started to increase and display an insulating R(T) behavior (see Fig. 2a). At lower temperatures near  $T^* = 3.6$  K, the insulating behavior changed to the metallic one. The former insulating R(T) curve near  $T_C$  can be understood with the Blonder–Tinkham–Klapwijk (BTK) theory, which considers the interfacial barrier effect at the N–S contact. According to BTK

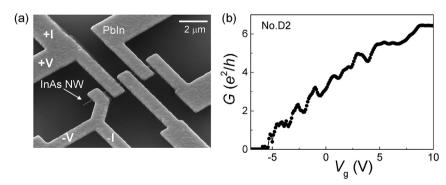
theory, the current flowing through the N–S interface is given by Ref. [16]

$$I_{NS} = \frac{1+Z^2}{eR_N} \int_{-\infty}^{\infty} \left[ f_0(E - eV) - f_0(E) \right] \times [1 + A(E) - B(E)] dE,$$
(1)

where Z is a parameter characterizing the height of a presumable tunnel barrier at the N–S interface (Z=0 for ideal transparency), V is the bias voltage,  $R_{\rm N}$  is the normal-state resistance,  $f_0$  is the Fermi–Dirac distribution function, A(E) is the probability of the Andreev reflection, and B(E) is the probability of the specular reflection. For  $E < \Delta$ , A(E) is given by  $\Delta^2/[E^2 + (\Delta^2 - E^2)(1 + 2Z^2)^2]$ , and B(E) is 1 - A(E). The R(T) curve near  $T_{\rm C}$  fitted well with the calculation result of  $(dI_{\rm NS}/dV)^{-1}$  using Z=2 and  $\Delta_0=1.14$  meV as fitting parameters, as shown in Fig. 2a. Here,  $\Delta_0$  is a superconducting gap energy of the PbIn electrode at zero temperature. The deviation between the calculation and experimental data occurring at lower temperatures is discussed later.

The differential conductance G=dI/dV was plotted as a function of V at the base temperature  $T=2.4\,\mathrm{K}$  (see Fig. 2b). The G(V) curve exhibited a ZBCP and additional peak structure at  $V_{\mathrm{gap}}=2.3\,\mathrm{meV}$ . The overall suppression of G below  $V_{\mathrm{gap}}$  was attributed to the formation of a non-ideal N–S interface, and the dI/dV peak position on the V axis corresponds to the superconducting gap voltage  $\Delta/e$ . Because there existed two N–S interfaces coupled in series via the InAs NW, the  $V_{\mathrm{gap}}$  value resulted in  $\Delta_{\mathrm{PbIn}}(2.4\,\mathrm{K})=1.15\,\mathrm{meV}$ , where  $\Delta_{\mathrm{PbIn}}$  is the superconducting gap energy of PbIn electrodes. This result is consistent with the fitting result of R(T) curve and other reports [14,17].

We note that the ZBCP diminished at a characteristic voltage of  $V^*=0.22$  mV. Increasing the lock-in bias voltage showed a similar suppression of the ZBCP, as shown in Fig. 2c. Because reflectionless tunneling arises from the quantum phase conjugation between the incident electron and Andreev-reflected hole, which traces back the path of the scattered electron, the characteristic voltage  $V^*$  for observing the ZBCP can be related to the Thouless energy  $E_{\rm Th}=eV^*=0.22$  meV of the InAs NW. Then, the phase coherence time is given by  $\tau_{\varphi}=\hbar/E_{Th}=3.0$  ps, which results in the phase-coherence length of  $L_{\varphi}=\sqrt{D\tau_{\varphi}}=205$  nm, where  $\hbar=h/2\pi$  is the reduced Planck's constant,  $D=v_Fl_m/3=140$  cm²/s is the diffusion coefficient, and  $v_F=1.04\times10^6$  m/s is the Fermi velocity [18]. Because  $L_{\varphi}$  is close to the channel length L=220 nm, we concluded that the whole NW segment between two PbIn electrodes contributes to the phase-coherent reflection tunneling to result in the observed ZBCP feature.



**Fig. 1.** (a) SEM image of the InAs NW device (D1) with the typical measurement configuration. The current bias I is applied between two PbIn electrodes (+I and -I) through the InAs NW, and the voltage V is monitored between the +V and -V electrodes. (b) Differential conductance G of sample D2 with the back-gate voltage  $V_g$  at T=10 K.  $V_g$  was applied to the Si substrate, and the source-drain bias voltage was  $V_{SD}=1$  mV.

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