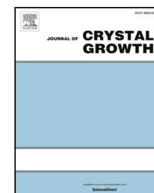
Journal of Crystal Growth 499 (2018) 90–97

Contents lists available at ScienceDirect

Journal of Crystal Growth

journal homepage: www.elsevier.com/locate/jcrysgro



In situ observation of crystal/melt interface and infrared measurement of temperature profile during directional solidification of silicon wafer

T.-J. Liao, Y.S. Kang, C.W. Lan*

National Taiwan University, Taiwan

ARTICLE INFO

Communicated by Pierre Müller

Keywords:
A1. Solidification
A1. Morphology
A1. Facet
A1. Temperature

ABSTRACT

The directional solidification of a (1 0 0) silicon wafer in ⟨1 0 0⟩ direction was carried out at various cooling rates. The planar to faceted melt/solid interfaces were observed, and the temperature profiles were measured by a mono-color pyrometer. The measured temperature profile for the planar interface is in good agreement with the analytical heat transfer model. Both undercoolings and thermal gradients in the melt and the crystal increased with the cooling rate, and the measured weighted thermal gradient $G*$ was also consistent with the classical morphological instability theory. Moreover, in addition to the facet evolution with the increasing growth velocity, the nucleation and growth of the facet layers appeared from the facet tip and formed bunching steps near the facet groove.

1. Introduction

Morphological development of the solid/melt interface during crystal growth is important, both fundamentally and technologically [1–5]. Especially, for the materials having large surface energy anisotropy, such as silicon, the transition from the planar to faceted interfaces [5–11], as well as pattern formation [12–15], have attracted much attention. The surface energy anisotropy, particularly the negative surface stiffness $\gamma + \gamma_{\theta\theta}$, plays a crucial role in the transition from wrinkling to sawtooth and coarsening; is the surface energy and the angle θ describes the deviation of the interface normal from some reference orientation [5,15]. According to the analysis by Norris et al. [5], the faceted interface might be stable even in absence of undercooling. As the undercooling reaches to a certain degree, the coarsening replaces the cell formation as the instability mechanism. Chen and Lan [15] also considered the negative surface stiffness for silicon in their phase field simulation of facet formation. The transition of planar to faceted interface occurred earlier than the prediction by Mullins and Sekerka's (MS) analysis [1–4,15]. In addition, although Chen and Lan [15] simulated the coarsening mechanism successfully, the facets remained stable only at low undercooling, about 0.1 K, in their simulation. Recently, the temperature gradient of the furnace was used to estimate the the undercooling on the faceted interface [16] and in the faceted groove [17]. The undercooling was up to about 4 K [16], but much smaller than 1 K due to twin nucleation [17].

In situ observations of the facet formation and coarsening during silicon crystal growth are important in getting a better understanding of the growth kinetics. Fujiwara et al. [8] was the first to develop an in situ observation system for silicon crystal growth. The infrared imaging was also used for temperature measurement. However, due to the poor resolution of the camera, the undercooling was not successfully measured. Moreover, the temperature gradients for crystal growth were too large, greater than 10 K/mm, so that the transition was not clearly observed as well. Tokairin et al. [9,13] further refined the previous experiments for ⟨1 0 0⟩ directional solidification of (1 0 0) Si wafers. A simple analytical heat transfer model was derived and the solutions indicated that the negative temperature gradient in the melt led to the sawtooth facets [9,13]. Beside the initial wavelengths of the facets were measured [9], the detailed facet unification mechanisms were further proposed [13]. The initial wavelength decreased with the increasing growth velocity, and this was consistent with the MS analysis [9]. Moreover, the stable spacing between facets after coarsening was found increased with the growth velocity, as well as the area of negative temperature gradients at the growth front [13]; the coarsening was due to the faceting kinetics [12]. However, because the temperature during crystal growth was not measured, the relationship of the morphological transition, coarsening, and faceting kinetics with the undercooling and thermal gradients remained unclear.

In this paper, we also setup an experimental system for the ⟨1 0 0⟩ directional solidification of (1 0 0) silicon wafer. The hot zone was carefully designed for better control of thermal gradients. Melting/solidification could be controlled by programed heating/cooling profiles

* Corresponding author.
E-mail address: cwlan@ntu.edu.tw (C.W. Lan).

https://doi.org/10.1016/j.jcrysgro.2018.08.004
Received 14 May 2018; Received in revised form 26 July 2018; Accepted 2 August 2018
Available online 03 August 2018
0022-0248/ © 2018 Elsevier B.V. All rights reserved.

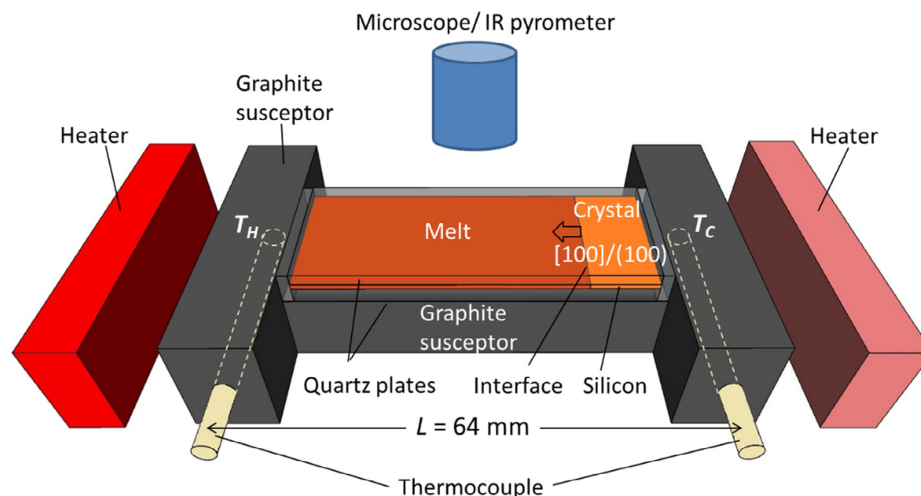


Fig. 1. In situ observation and temperature measurement setup for directional solidification of silicon wafer.

with a fixed thermal gradient. In addition to the observation of the interface morphology, the temperature was also measured using a mono-color pyrometer with a spot size of 0.35 mm. The undercooling and the thermal gradients were estimated from the infrared (IR) measured temperature profiles after calibration. Because the developed facets were significantly bigger, 1–2 mm, than the previous study, the detailed step formation from the facet tip and the bunching steps near the facet groove were also observed for the first time.

2. Experimental

2.1. System setup

The experimental setup is similar to the one used by Tokairin et al. [9,13], but with a different hot zone design for better control of thermal gradients. The schematic of the system is shown in Fig. 1. As shown, the silicon sample, a 0.85 mm × 10 mm × 26 mm boron-doped Cz (1 0 0) silicon wafer, was placed between two quartz plates; the resistivity of silicon was 20 Ohm-cm. The upper plate (2 mm thick) was polished on both sides, while the lower plate (3 mm thick) was not polished having a foggy surface for better wetting with silicon melt. Before the experiment, the quartz parts were cleaned by immersion in a solution of 1 vol % HF and 0.5 V% HCl for 5 min. Silicon samples were also cleaned using 1 vol% HF for 5 min. This sandwich sample was then surrounded by polished quartz bars to prevent the silicon melt from leakage during experiment. The growth cell was placed upon the graphite susceptor, whose both ends were connected to graphite blocks. Each block had a B-type thermocouple inside for temperature control. The graphite blocks were heated by two graphite heaters. To prevent heat loss and facilitate the directional melting and solidification, graphite felt was used for insulation. The upper insulation had a small hole for observation and IR temperature measurement.

At the beginning of the heating process, the furnace was vacuumed ($\sim 2 \times 10^{-4}$ Pa) and flushed with high purity argon. The hot-zone temperature T_H was set at a temperature higher than the melting point of silicon T_m, while the cold-zone temperature T_C was lower than T_m. The melting process was controlled through heating, but the temperature difference ΔT, i.e., T_H-T_C, was kept the same being about 200 K. This gave a temperature gradient of about 3.1 K/mm; the distance between two thermocouples was 64 mm. As temperatures rose to certain values, silicon started to melt. When the melting front was under the view window, we could observe the melt showed up moving from one end of the wafer to the other. To prevent the seed from completely melting, the heating needed to be stopped at certain temperatures. After the sample reached a steady state, we reversed the process for crystal growth. During cooling, the crystal/melt interface could be observed again and it moved along the ⟨1 0 0⟩ direction from the right to the left.

The temperature profiles for the melting/growing process in Exp. A (the case having a planar growth front) are showed in Fig. 2(a). The IR measured temperature profile was also shown; the emissivity ε was set to 0.6 in the pyrometer at the beginning. The temperature calibration will be discussed shortly. As shown, as the interface passed through the IR spot, there were step changes in the signal. This was due to the different emissivities of the melt and the crystal; the melt emissivity was significantly lower. The observed images of the melting/growing interfaces in Exp. A are showed in Fig. 2(b). During melting, the interface was always planar (top figure). However, during crystal growth, the interface could be planar or faceted depending on the cooling rate. In the present case (Exp. A), the growth interface was planar. In addition, the IR spot size was about 0.35 mm, as indicated by the red[1] spot in Fig. 2(b). This could also be checked easily from the width or elapsed time of the step changes in the IR signal in Fig. 2(a); the interface velocity multiplied by the elapsed time was about the spot size.

This melting/growing process was repeated for three times. The first time was to observe the interface morphology by a digital microscope (KEYENCE, VHX-2000). The 2nd time was to measure the temperature profile through a mono-color IR pyrometer (SENSORTHERM, Model MS09). The final time was to ensure the variation of average growth velocities was within 6% as compared with the first time.

2.2. Temperature calibration

As just mentioned, the IR temperature in Fig. 2(a) had step changes when the melting/growing interface passed through the IR spot, and this was due to the much lower emissivity in the melt than that in the solid, as shown in Fig. 2(b). Moreover, the measured IR temperature during melting was not the same as the melting point of silicon, 1683 K. Therefore, it would be necessary to convert the IR reading into the real temperature. The calibration procedure was rather straightforward.

Firstly, we needed to extract the melting point of silicon from the IR measured profile during the melting stage, which had no undercooling or superheating. As shown in Fig. 3, we found a vertical line at the middle of the first step change. Then, we extrapolated the temperature from the solid side at the point slightly outside the IR spot, i.e., the width of the step change, to intersect the vertical line. This was to make sure that silicon remained all solid inside the IR spot, and had no

[1] For interpretation of color in Figs. 2, 6, 8, the reader is referred to the web version of this article.

Download English Version:

https://daneshyari.com/en/article/8148361

Download Persian Version:

https://daneshyari.com/article/8148361

Daneshyari.com