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Porous silicon reorganization: Influence on the structure, surface roughness and strain

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ABSTRACT

Porous silicon and epitaxial thickening is a lift-off approach for silicon foil fabrication to avoid kerf losses and produce foils with thicknesses less than 50 μm. The crystal quality of the epitaxial silicon film strongly depends on the porous silicon template, which can be adapted through a reorganization process prior to epitaxy. In this work, we investigated the influence of reorganization on the structure of etched porous silicon layers. The reorganization processes were carried out in a quasi-inline Atmospheric Pressure Chemical Vapor Deposition reactor. Variations on the temperatures and process durations for the reorganization step were examined. The cross-sections showed that porous silicon requires temperatures of approximately 1150 °C to produce an excellent template for epitaxy. Atomic Force Microscopy measurements on the samples annealed at different temperatures showed the evolution of the pores from as-etched to a closed surface. These measurements confirm that the surface is not yet closed after 30 min of reorganization at 1000 °C. Different durations of the reorganization step at a fixed temperature of 1150 °C all lead to a closed surface with a comparable roughness of less than 0.5 nm. X-ray diffraction measurements show a change in the strain in the porous layer from tensile to compressive when the reorganization temperature is increased from 800 °C to 1150 °C. A longer reorganization at a fixed temperature of 1150 °C leads to a reduction in the strain without reducing the quality of the surface roughness. Defect density measurements on silicon layers deposited on those templates confirm an improvement of the template for longer reorganization times. This study shows that our porous silicon templates achieve lower surface roughness and strain values than those reported in other publications.

1. Introduction

Processes using porous silicon and epitaxial thickening for the production of thin silicon devices have already been successfully transitioned from microelectronic to photovoltaic (PV) applications [1,2]. For this approach, a stack including a low porosity top layer and a high porosity layer is electrochemically etched onto a silicon substrate. The etching process will not be discussed in detail, as it is well described in literature [3,4]. During a high temperature anneal, the high porosity layer forms a separation layer containing large cavities, which allows the detachment of the epitaxially grown foil from the reusable substrate. Simultaneously, the top region of the low porosity layer reorganizes to a closed surface, which serves as a template for epitaxy. Most research on enhancing the detached silicon foil quality has been performed by the Interuniversity Microelectronics Centre (IMEC) and focused on adapting the porous silicon etching process. The aim was to minimize the surface roughness and strain in the porous silicon template after annealing by adjusting the porous silicon layer thicknesses and porosities [5–7].

In the case of two-layer porous silicon stacks, a trade-off between the layer roughness and strain has to be made. The root mean square (RMS) roughness increases for longer annealing times, whereas the out-of-plane strain is reduced. RMS roughness values as low as 2 nm could be reached for a double porous silicon layer with a low porosity layer thickness of 1300 nm and an annealing time of 1 min. The out-of-plane compressive strain in this layer for the same annealing time is 1.6×10^{-4}. For an annealing time of 30 min, the strain can be reduced to 1.2×10^{-4}, which results in an increased RMS value of 12 nm [6]. This trade-off can only be avoided using a new triple layer stack, which features two low porosity layers on top of one high porosity layer [8]. Radhakrishnan et al. state that the first thin (approximately 100 nm), low porosity layer located at the growth interface is needed to achieve a good template and the second low porosity layer is needed to ensure easy detachment. The main disadvantage of this new layer stack is an increase in the required etching time of approximately 25–40%. Unfortunately, no publications are

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available that show surface roughness and strain values for this new triple layer stack.

In this work, only the reorganization process, which restructures the porous layers prior to epitaxy is investigated using commercially available microelectronics material featuring one low porosity layer on top of two high porosity layers. This three layer stack is based on a double layer stack optimized for ultra-thin chip fabrication. Details of the layer stacking and the etching process are found in Refs. [9,10]. The third high porosity layer was introduced by IMS to guarantee detachment of a larger area. The advantage compared to the triple layer introduced by Radhakrishnan et al. is that the process time increases only slightly as a result of etching the second high porosity layer. In this paper, we want to achieve comparable or better template qualities with this commercially available material. The aim was to find the required temperature regime that would enable an optimized reorganization of the porous structures. The evolution of the pores during reorganization is discussed. In Ref. [11], the authors describe the start of reorganization at 880 °C for a porous silicon monolayer. Therefore, temperature variations over the range from 800 °C to 1150 °C are examined in this work to resolve the different stages from an as-etched to a closed surface during the reorganization process. In previous works, improvements in the material quality for an increased reorganization time at 1150 °C were observed [12]. For this reason, the annealing duration for a fixed temperature of 1150 °C was varied to investigate whether a longer reorganization time leads to a reduction in the strain within the layer, as is expected from [6]. Additionally, defect densities were measured on 40 μm thin silicon layers that have been epitaxially grown on porous silicon after reorganization at 1150 °C for different time durations.

2. Experimental

Porosified 6 in. p-type Cz substrates with a specified resistivity of 10–20 mΩ*cm were supplied by IMS (Institut für Mikroelektronik Stuttgart). Their porous layer consists of a 1.4 μm thick low porosity (20–30% porosity) layer on top of two high porosity layers (50–60% porosity) with differing porosities and 400 nm each in thickness. Prior to processing, all samples were etched in 1% HF (aq) to remove the grown native oxide and enable a reproducible reorganization result [12]. All experiments were carried out using a lab-type quasi-inline Atmospheric Pressure Chemical Vapor Deposition (APCVD) reactor [13]. To investigate the pore evolution in the porous silicon layer and in more detail the surface, which acts as a template for epitaxial growth, the samples received a reorganization step in a hydrogen atmosphere without any additional epitaxial growth of a silicon layer. The samples were reorganized at different temperatures for 30 min and for different time durations at a fixed temperature of 1150 °C, respectively. The heating ramp was set at 100 °C/min for all processes. To gain information about the influence of the most promising templates on the epitaxial layer quality, 40 μm thin silicon layers were grown on porous silicon after reorganization at 1150 °C for different time durations. All samples with an epitaxial layer were Secco[1] etched for 40 s before defect density measurements have been conducted. An overview of the different processes in this work is given in Table 1.

The reorganized porous structures were observed using a scanning electron microscope (SEM). The cross-sections were prepared by manually scribing and breaking the samples. The surface roughness was determined using an atomic force microscope (AFM) using a Tap300DLC probe in tapping mode. X-ray diffraction (XRD) measurements on the same layers were conducted using a Philips X'Pert MRD system equipped with a CuK_α X-ray ($\lambda = 0.154$ nm) source. To extract the strain in the porous layer from the XRD measurements, the silicon and porous silicon peaks were both fitted to Gaussian functions to determine the corresponding scattering angle θ_B. Using Bragg's law of diffraction, which is defined as:

$$2 \cdot d \cdot \sin \theta_B = n \cdot \lambda \quad (1)$$

the lattice parameter d of the porous silicon layer and the silicon substrate can be calculated using for λ the known wavelength of the CuK_α X-ray source. The relative deformation ε_s of the porous silicon layer (PS) on the silicon substrate (Si), also known as the out-of-plain strain, can then be calculated via the mismatch between the two lattice parameters:

$$\frac{d_{PS} - d_{Si}}{d_{Si}} = \varepsilon_s. \quad (2)$$

Table 1
Overview of the different reorganization parameters varied in this work.

Process	Process temperature [°C]	Reorganization time [min]	Subsequent growth of a 40 μm silicon layer
A	800	30	
B	950	30	
C	1000	30	
D	1150	30	
E	1150	10	
F	1150	5	
G	1150	30	✓
H	1150	5	✓

3. Results and discussion

3.1. A.Porous silicon layer structure and surface roughness

This section discusses the structure of the layers after processing and the surface roughness determined using SEM and AFM, respectively. The aim was to determine the optimum temperature regime to achieve excellent reorganization results for a closed and detachable template for epitaxial growth. This reorganization process should require 1–30 min., and be transferable to industrial in-line CVD reactors.

3.1.1. Dependence on temperature

Annealing the porous layers at 800 °C for 30 min caused a change in the structure compared to the as-etched sample (Fig. 1) when examined using SEM. The long pore tubes separate and become small closed pores with a diameter in the range of a few nanometers. The 800 nm thin, high porosity layers can now be better distinguished from the low porosity layer. The growth of larger pores and the shrinking of smaller pores during annealing is well explained by the theory of sintering [11,14]. It states that the reorganization of porous silicon occurs through vacancy diffusion processes. They are evoked through a vacancy concentration gradient between the pore and its surrounding lattice. Voids can therefore grow or shrink depending on the direction of this vacancy gradient [7]. Ott et al. [11] state that increasing the annealing time for a constant temperature leads to a similar evolution in the pore structure, as an increase of the annealing temperature. Any further increases to the annealing time may

[1] Secco-etch: $HF + K_2Cr_2O_7 + H_2O$ in a ratio of $HF:H_2O = 2:1$ with 44 g $K_2Cr_2O_7$ dissolved in 1 l of H_2O. It etches defects on all surfaces.