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Wire or no wire—Depends on the catalyst layer thickness

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ABSTRACT

Crystalline silicon (Si) nanowire could be directly grown from Si wafer upon thermal annealing in the presence of catalyst such as gold (Au). However, the role of the catalyst layer thickness is yet elucidated. In this work, 10 nm, 20 nm, and 40 nm Au layers were respectively sputtered on Si wafer substrates, followed by 2 min thermal annealing at 1000 °C under Ar atmosphere, to find the relationship between the catalyst layer thickness and formation of the nanowire. Results show that in the case of thin layer of catalyst, crystalline-Si/amorphous-SiO_x coaxial nanowires grew. But with thicker layers of catalyst, no wires were found but crystalline Au particles capsulated with amorphous SiO_x. The catalyst and nanowire morphologies and structures were carefully examined through a scanning electron microscope, X-ray diffraction, transmission electron microscopy, energy dispersive X-ray spectroscopy and selected area diffraction. A model is developed to explain the formation mechanism of the Si/SiO_x and Au/SiO_x core–shell nanostructures.

1. Introduction

Crystalline silicon (Si) nanowires are important building blocks in semiconductor devices [1–4], Crystalline-Si/amorphous-SiO_x, or c-Si/a-SiO_x, coaxial nanowires are reported to be grown by laser ablation [5], chemical vapor deposition [6,7]; thermal degradation of diphenylsilane in a supercritical hexane fluid [8], thermal evaporation [9], or thermal annealing of metal-covered Si wafers [10–13]. Among them, the thermal annealing method follows a solid–liquid–solid (SLS) growth mechanism [14,15]. The SLS growth of c-Si/a-SiO_x and a-SiO_x nanowires grown from different metallic catalyst layers has been reported in a few papers. For instance, c-Si/a-SiO_x nanowires are grown via thermal annealing of Si wafers covered by a 1-nm Fe film [11], 10-nm Au film [13,16], 40-nm [17], or 50-nm Ni film [18]. Amorphous SiO_x (i.e., the oxidized Si) nanowires are grown via thermal annealing of Si wafers covered by 2–10 nm Au film [19], 5-nm Pt film [15], 15-nm Pt/Au film [20], 30-nm [21], or 40-nm Ni film [14]. Till now, however, how the metallic catalyst layer thickness affects the growth of c-Si/a-SiO_x or a-SiO_x nanowires is yet elucidated. In this work, thermal annealing was carried out on Si wafers coated by 10-nm, 20-nm, and 40-nm Au layers to study if they all grow nanowires. The results show that the thin layers do but thick layers do not. Scanning electron microscope, X-ray diffraction, transmission electron microscopy, energy dispersive X-ray spectroscopy and selected area diffraction patterns were employed to examine the resultant morphology and structure. A solid–liquid–solid model was developed to explain the formation mechanisms.

2. Experimental details

2.1. Deposition of Au layers

Au catalyst layers were sputtered on Si wafers in an auto fine coater (JFC-1600, JEOL, Japan), consisting of a basic unit and a rotary pump. The cathode contains a permanent magnet to create an efficient glow discharge for sputtering. N-type Si (100) wafer was used as the substrate (10 mm × 10 mm in area, 475 μm in thickness and 0.5 nm in room mean square surface roughness). Before loading into the sputtering chamber, the substrate was ultrasonically cleaned in acetone for 20 min, followed by 10 min in alcohol. Once the chamber pressure reached around 10 Pa, 0.5, 1, and 2 min sputtering of an Au target (purity, 99.99%) at room temperature deposited about 10-nm, 20-nm, and 40-nm-thick Au catalyst layers on the Si wafer substrates.

2.2. Growth of Si nanowires

The as-sputtered Au layers underwent thermal annealing in an advanced rapid thermal system (ARTS150, Premtek international

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Inc., Taiwan, China) in an Ar ambient at 1000 °C for 2 min. The annealing chamber was purged with Ar (purity, 99.999%) at 3000 standard cubic centimetres per minute (sccm) for 15 min before ramping up to 1000 °C at 50 °C s^{-1}. And then, the chamber was held at 1000 °C for 2 min. After the annealing, the chamber was naturally cooled down to room temperature for about 60 min. During the whole annealing process (ramping, dwelling, and cooling), the inflow of the Ar gas was maintained at 3000 sccm.

2.3. Characterization

Field emission scanning electron microscopy (JEOL, JSM-6701F, JEOL Ltd., Japan, 10-kV operating voltage) was employed to observe the cross section and the surface morphology of the Au catalyst layers before and after annealing. The polycrystalline structure of the as-sputtered Au film was examined by glancing incidence X-ray diffraction (PANalytical B.V., Almelo, Netherlands). High resolution transmission electron microscope (TEM, JEOL 2010, 2100, 200-kV operating voltage, Japan) was employed to reveal the morphology and structure of the grown nanowires and particles. Energy dispersive X-ray spectroscopy (EDX, EDAX Inc., US) is applied to characterize the composition of the nanowire and particles. Selected area electron diffraction (SAED) patterns were carried out to characterize the growth orientations of the grown nanowires and particles. In determining the growth orientations, the SAED patterns were generated by carefully adjusting the tilt angle along the *x*- and *y*- axis of the sample holder to match the standard database that is cited from software JEMS (cf., Supporting database).

3. Results and discussion

3.1. Morphology and structure of the Au catalyst layers

3.1.1. As-sputtered Au layers

The cross section of the as-sputtered Au layers with thickness of 10 nm, 20 nm, and 40 nm is clearly shown in Fig. 1(a)–(c). The rougher surface of the 10-nm thick Au layer may be resulted from the attachment of the small broken Si pieces during cutting the sample. Fig. 1d shows that the 40 nm Au layer surface is uniformly covered with small Au nanoparticles with diameter of around 10 nm. The XRD spectrum generated from the 40-nm Au layer is shown in Fig. 1e, where six characteristic peaks: (111) centered at 38.3°, (200) centered at 44.6°, (220) centered at 64.7°, (311) centered at 77.6°, (222) centered at 82.4°, and (400) centered at 98.1° are detected, exhibiting the typical face-centered cubic (FCC) crystalline structure of Au (cf., PDF# 00-001-1172, Supporting data 1).

3.1.2. Annealed Au layer surfaces

Upon 2-min thermal annealing, nanowires are found lying on the surface of the Si wafer coated with 10-nm Au layer (cf., Fig. 2a). The wires entangling with each other are of around 70 nm in diameter, several microns in length. Small Au nanoparticles with diameter of around 70 nm are also clearly seen on the Si wafer seeding the growth of the nanowires (cf., Fig. 2a, dark arrow). However, no nanowires are found on the Si wafer covered with 20-nm Au layer, except for the micron-sized Au particles with diameter in the range of 150–524 nm (cf., Fig. 2b). A 68-nm-diameter particle is occasionally observed (cf., Fig. 2b, dark arrow). The formation of the particles is attributed to the effect of surface tension at high temperature. As the Au layer thickness increased to 40-nm, bigger particles with diameter ranging from 281 nm to 722 nm are found. Small particles with diameter of around 104-nm are occasionally observed (cf., Fig. 2c, dark arrows). Small amount of nanowires with diameter of 28–48 nm, and length of around 3 μm, are occasionally found on the surface. They are not directly seeded by the big Au particles, but by the small ones that are collapsed from the big ones (cf., Fig. 2d, dark arrows). It is also noted that all the big particles are shielded by a layer of white matter (cf., Fig. 2d, white arrows). It is known that the Au particles collapsed from the Au layers could easily melt with Si wafer because the eutectic point of the Au–Si alloy is only 363 °C [22]. Since the commercial argon gas usually contains a small amount of

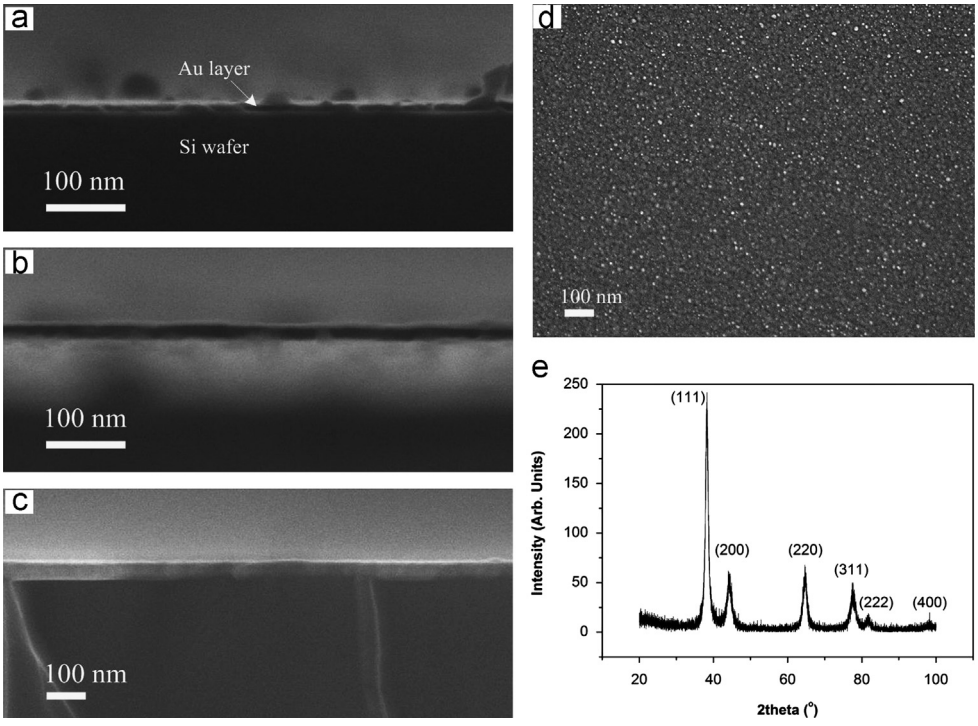

Fig. 1. Morphology and structure of the as-sputtered Au catalyst layers: (a) 10 nm, (b) 20 nm, and (c) 40 nm. (d) Surface morphology of the 40 nm Au layer. (e) X-ray diffraction patterns generated from the 40 nm Au layer.