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Growth of silicon carbide epitaxial layers on 150-mm-diameter wafers using a horizontal hot-wall chemical vapor deposition

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ABSTRACT

Epitaxial layers on a 150-mm-diameter silicon carbide wafer have been grown using a horizontal hot-wall chemical vapor deposition system for three 150-mm-diameter wafers. We investigated the surface morphology and surface defects such as shallow pits and triangular defects of the grown epitaxial layers, as well as the thickness and carrier concentration uniformities. The shallow pit and triangular defect densities were 4.6 cm^{-2} and 1.6 cm^{-2}, respectively, and the thickness and the carrier concentration uniformities were 3.9% and 47%, respectively. We focused on improving the carrier concentration distribution for practical use and concluded that the cause of the distribution was the distribution in the effective C/Si ratio in the direction of the gas flow.

1. Introduction

Power devices are used to control various high-voltage components such as power supplies and motors so that electricity can be used efficiently. Silicon carbide (SiC) possesses certain physical properties such as a wide bandgap and high thermal conductivity that allows high-temperature operation and miniaturization of power devices, which in turn expands the range of use such power devices and creates space for other functional systems. Therefore, it is expected that SiC power devices are often used for applications such as automotive and railway electronics. SiC power devices such as Schottky barrier diodes and metal-oxide-semiconductor field-effect transistors (MOSFETs) are commercially available. However, because these devices are more expensive than common Si-based devices, it is necessary to reduce the cost of chips to further expand their use. The mainstream SiC wafer sizes are 75 and 100 mm diameter, but larger wafers will result in a reduction of the chip cost because a larger number of chips per wafer area can be fabricated. Indeed, Si wafer sizes have been enlarged to improve the productivity, and wafers with diameters of up to 200 mm are already used for power devices.

SiC wafers with a 150-mm diameter should be used from now on because such wafers are becoming standard materials in the industry. Some vendors have already released 150-mm-diameter SiC bulk wafers [1], and growth of SiC epitaxial layers on such wafers has been reported [1,2]. Burk et al. first reported SiC epitaxial layer growth on 150-mm-diameter wafers using a planetary chemical vapor deposition (CVD) system in 2012 [1]. They achieved a total defect density of 4.4 cm^{-2} and thickness and carrier concentration uniformities of 1.6% and 12.8%, respectively. Miyasaka et al. also reported SiC epitaxial layer growth on 150-mm-diameter wafers using a planetary CVD system, but the carrier concentration uniformity was of an undesirable level [2]. To obtain SiC epitaxial layers on 150-mm-diameter with a suitably high quality, conditions relating to the defect density and carrier concentration uniformity have not yet been satisfied.

The surface morphology, shallow pits, and triangular defects of SiC layers should be investigated because they have an adverse influence on the performance of SiC-based devices [3–8]. It has been reported that a rough surface and shallow pits, which originate from threading screw dislocations, degrade the reliability of gate oxides [3,6,7]. Moreover, triangular defects have been reported to be one of the main causes of short MOS capacitor

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lifetimes [8]. In addition, there are no reports on shallow pits that consider the whole wafer because it is difficult for conventional optical surface analyzers to detect shallow pits.

The thickness and carrier concentration uniformities of the epitaxial layers are also important because they have a significant effect on device yields. In general, the type of growth system affects the uniformities, and therefore, the uniformities obtained with each growth system need to be investigated.

We have previously grown SiC epitaxial layers with a size equivalent to 150 mm by arranging two wafers with 75-mm diameters and using a horizontal hot-wall CVD system for three 150-mm-diameter wafers, Tokyo Electron Probus-SiC [9]. We focused on the surface morphology and surface defects such as shallow pits and triangular defects of these layers and found that the C/Si ratio is an important growth parameter for improving the surface morphology and reducing the surface defect density.

In this study, we grew an epitaxial layer on a 150-mm-diameter wafer using the horizontal hot-wall CVD system and investigated the surface morphology, surface defect density, and thickness and carrier concentration uniformities. To do this, we first grew epitaxial layers with an equivalent 150-mm-diameter size to optimize the growth conditions for a smooth surface and few surface defects over the whole wafer. We discuss here the origins of the carrier concentration distribution and way to improve the uniformity.

2. Experimental procedure

Epitaxial growth was performed using a horizontal hot-wall CVD system, Tokyo Electron Probus-SiC. Fig. 1(a) and (b) show schematic drawings of the CVD reactor from parallel and perpendicular to gas flow directions, respectively. The fixed susceptor, which is heated by a high-frequency induction heating system, and rotary susceptor are made of graphite. A wafer holder for three 150-mm-diameter wafers is placed on the rotary susceptor during growth. A schematic drawing of the wafer holder is shown in Fig. 1(c). Open circles and dashed circles show the wafer pockets with 150 mm diameter and 75 mm diameter, respectively. The off-angle direction is the same as the rotation tangential direction when wafers are put on the wafer holder as shown in this figure. Two wafers with diameters of 75 mm are arranged in the radial direction of the wafer holder to grow layers with an equivalent 150-mm-diameter size.

Conventional *n*-type 4H-SiC Si-face wafers with a 4° off-angle toward the [11–18] direction were used as substrates after chemical-mechanical polishing treatment. In-situ H_2 etching was carried out at 1605 °C and 12 kPa. The H_2 flow rate was 150 slm, and the etched depth was about 55 nm. Epitaxial layers were grown for 1 h. The growth temperature was varied between 1580 and 1680 °C, and the growth pressure was varied between 6.3 and 12 kPa. N_2 as a doping gas was injected at a rate of 5 sccm. The H_2 and C_3H_8 (10% in H_2) flow rates were 100 slm and 170 – 230 sccm, respectively. The C/Si ratio was changed from 1.0 to 1.8 by varying the flow rate of SiH_4 (10% in H_2). The growth rate was about 5.5 μm/h.

The thickness and carrier concentration were investigated by using conventional Fourier transform-infrared spectroscopy and mercury probe capacitance–voltage measurements, respectively. The surface morphology and surface defects were inspected by using a confocal microscope with a differential interference contrast (CDIC) system, Lasertec SICA 61. The confocal microscope system efficiently obtains signals from the surface because out-of-focus signals are rejected, and using the SICA therefore enables shallow pits to be detected. Reflection loss was detected to investigate the surface morphology throughout the whole wafer and was estimated from the difference between the irradiated and reflected light intensities. Large reflection loss values mean that the reflected light intensity decreased due to a rough surface.

3. Results and discussion

3.1. Growth of SiC epitaxial layers with an equivalent 150-mm-diameter size

We began by growing epitaxial layers with an equivalent 150-mm-diameter size to optimize the growth conditions for a 150-mm-diameter epitaxial layer. The surface morphology and densities of surface defects such as shallow pits and triangular defects were investigated across the whole wafer.

Fig. 2 shows the dependence of the reflection loss on the C/Si ratio; the reflection loss was obtained from SICA measurements of the two 75-mm-diameter wafers. The reflection loss of a conventional epitaxial layer with an 8° off-angle, which has smooth

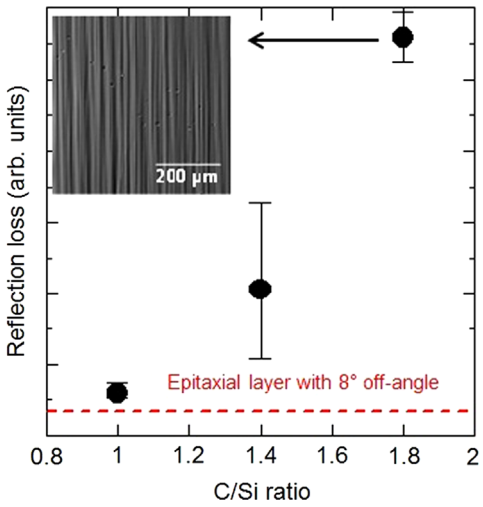

Fig. 2. Dependence of the reflection loss on the C/Si ratio. (Inset: CDIC image of the epitaxial layer grown at a C/Si ratio of 1.8.)

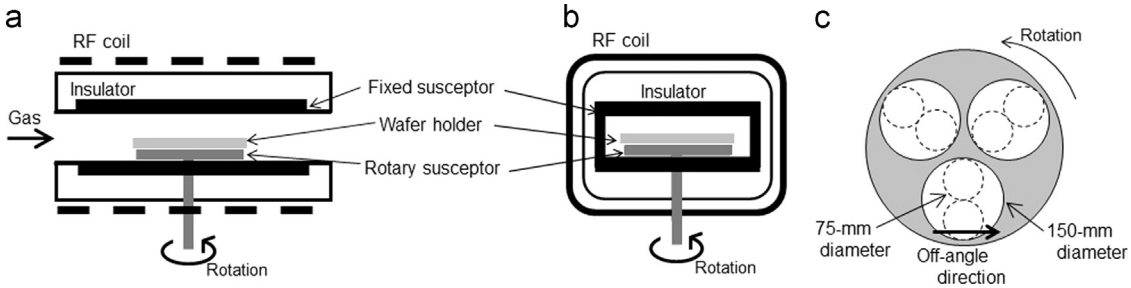

Fig. 1. Schematic drawing of the (a) CVD reactor and (b) wafer holder. The wafer pockets have diameters of 150 mm (solid lines) and 75 mm (dashed lines).