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Comparison of the effects of 60 nm and 96 nm thick patterned permalloy thin films on the performance of on-chip spiral inductors

Vasu Pulijala*, Azeemuddin Syed

CVEST, IIIT Hyderabad, Gachibowli 500032, Hyderabad, India

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ABSTRACT

In our earlier work it was shown that the 60 nm domain patterned Permalloy, incorporated on on-chip spiral inductors, gave better performance at frequencies greater than 5 GHz compared to the bulk Permalloy incorporated inductors, and the control structure. In this paper we compare the effects of 60 nm and 96 nm thick domain patterned Permalloy thin films, on the performance of on-chip spiral inductors. Experimental results show that the 60 nm thick both bulk and patterned Permalloys provide more improvement in inductance and quality factor of inductors, compared to that of 96 nm.

1. Introduction

In research related to magneto-electronic applications, it was observed in Permalloy thin film patterns that cross tie walls exist between 40 nm and 70 nm thickness and the transition from cross-tie to asymmetric bloch wall occurs between 70 nm and 100 nm thickness [1]. It is established that the formation of domain walls in Permalloy patterns is dependent on the thickness of the thin film [1,2]. In another work it was shown that demagnetization energy and hence the stray fields associated with Permalloy patterns with similar shapes, vary with the type of domain walls formed [3].

Passive inductors which occupy least area and provide higher performance in terms of inductance, quality factor, and better high frequency response, are essential for monolithic radio frequency integrated circuit(RFIC) design. Employing magnetic materials with on-chip inductors in RFICs is a widely used approach to improve their performance. Few researchers have synthesized new magnetic materials [4–10], while others used Permalloy [11–14]. Compared to bulk films, when laminated or patterned magnetic films are employed, improvement in high frequency response is observed [11–17].

Permalloy is a soft magnetic material and compatible with CMOS technology. It could be observed that significant number of the researchers employed Permalloy with thicknesses ≥100 nm with inductors. In one of the works, it was shown that the 60 nm laminated rings of Permalloy have improved the performance of the inductor compared to higher thickness laminations [14]. But the frequency response was limited to around 1 GHz. It was also shown that the permeability of 60 nm thin film Permalloy is higher than 80 nm and 100 nm thicknesses [14,18].

In our earlier work the effect of controlled formation of Permalloy($Ni_{80}Fe_{20}$) domains [19,20], on the performance of on-chip planar spiral inductors was presented. It was also shown that the 60 nm domain patterned Permalloy when incorporated with on chip spiral inductors gave better performance at frequencies greater than 5 GHz. In these works the necessity of incorporation of appropriate domain pattern and its orientation for high frequency applications was elucidated.

In this paper we compare the effects of 96 nm thick Permalloy patterns, which are likely to have asymmetric bloch walls, and 60 nm thick patterns, which are likely to have cross-tie walls, on the inductance and quality factor of inductors. Object Oriented Micromagnetic Framework (OOMMF) [21] simulations have also been performed on Permalloy patterns with same thicknesses, but with smaller sizes than the fabricated patterns due to computational constraints. The domain walls formed and the energy components of these patterns are analyzed using OOMMF simulations.

2. Experiment

Planar spiral inductors, which have 15 μm wide aluminum lines, spacing of 15 μm and 2.75 turns are fabricated with 200 nm thick aluminum. These conductive lines are deposited on top

* Corresponding author.
E-mail address: vasu.pulijala@research.iiit.ac.in (V. Pulijala).

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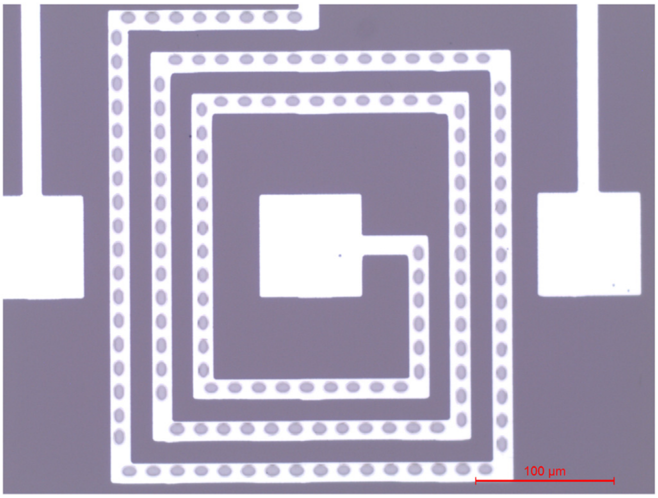

Fig. 1. Fabricated inductor with Permalloy patterns of size 8 µm × 11 µm × 96 nm.

of 1 µm thick silicon dioxide with a n-type doped silicon substrate, on two separate wafers. The n-type doped silicon substrate has an average conductivity of 25 S/m.

Permalloy patterns of various sizes are DC sputter deposited on top of aluminum lines as shown in Fig. 1. Base pressure of the vacuum system is 6.77E−6 Torr and Permalloy is deposited in a 6.32E−3 Torr Argon ambiance. A 100 W DC power is used for the deposition. Detailed fabrication steps could be found elsewhere [20]. 60 nm thick Permalloy patterns with maximum variation of 3 nm thickness are deposited on top aluminum on the first wafer. 96 nm thick Permalloy patterns with maximum variation of 4 nm are deposited on the second wafer.

An inductor with bulk Permalloy running on top of aluminum lines (Fig. 2), and a control structure without any magnetic material are also fabricated on both the wafers. It is ensured that both wafers are subject to similar temperature, pressure and ambient conditions when oxidizing, and while sputtering aluminum and permalloy.

Inductors used in this work do not have an underpass. In order to measure the properties of inductors a bond pad is added at the center of inductor as shown in Fig. 1.

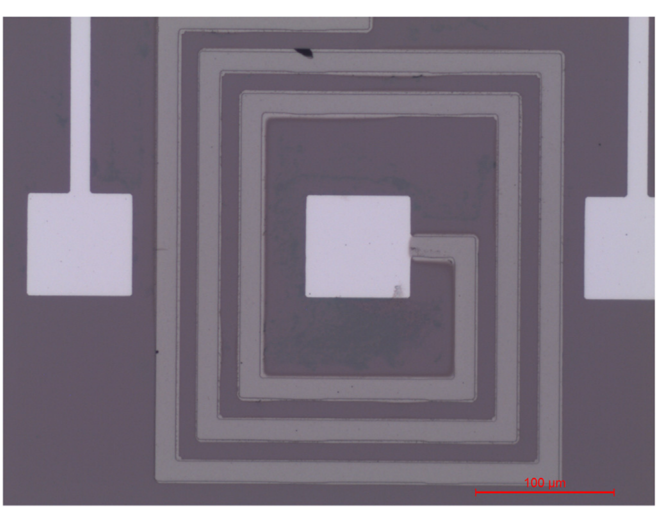

Fig. 2. Fabricated inductor with 96 nm thick bulk Permalloy on top of Aluminum.

3. Results

Inductance and quality factor of the fabricated inductors are obtained from the *S*-parameters measured from 100 MHz to 20 GHz using Agilent E8361A Performance Network Analyzer. Open bond pad structure's scattering parameters are also measured for de-embedding. Admittance (*Y*) parameters of open bond pad structures and spiral inductors are derived from the measured *S*-parameters. *Y*-parameters of the open bond pad structures have been deducted from the *Y*-parameters of the inductors, to obtain the de-embedded admittance parameters of spiral inductors alone without bond pads. Using the de-embedded *Y*-parameters, equivalent inductance (*L*) and quality factor (*Q*) are obtained as follows:

$$L = \frac{Imag(\frac{-1}{Y_{12}})}{2\pi f} \tag{1}$$

$$Q = -\frac{Imag(Y_{12})}{Real(Y_{12})} \tag{2}$$

8 µm × 11 µm × 60 nm patterns gave highest inductance after 5 GHz. It could be observed that both the bulk and patterned 60 nm thick Permalloy have given higher improvement in inductance compared to the 96 nm thick Permalloy. Till 5 GHz, inductor with 60 nm bulk Permalloy gave highest inductance. The inductances extracted are shown in Fig. 3. Peaking of inductances around 10 GHz is because of the capacitive coupling with conductive silicon substrate. 60 nm Permalloy patterns gave better boost in quality factor compared to 96 nm Permalloy as shown in Fig. 4.

Though Permalloy patterns with various shapes and sizes are fabricated on both the wafers only significant results are reported here. It is re-emphasized here that not all 60 nm patterns gave higher improvement in inductance signifying the importance of choosing appropriate domain patterns defined by the shape of patterns.

Table 1 shows the peak inductance and quality factors of 8 µm × 11 µm patterns. There is a decrease in inductance after 10 GHz for the control structure. It could be observed that the

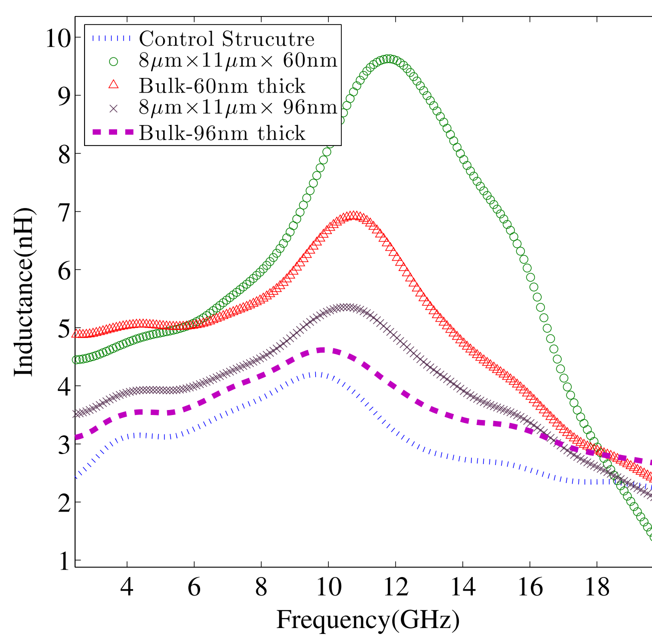

Fig. 3. Inductance of the spiral inductors with patterned Permalloy, Bulk Permalloy (60 nm and 96 nm thick) and without Permalloy.