Physica B: Condensed Matter 538 (2018) 104–108

Contents lists available at ScienceDirect

Physica B: Condensed Matter

journal homepage: www.elsevier.com/locate/physb

Features of changes in electrophysical properties of silicon under the influence of thermal treatment

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ARTICLE INFO

Keywords:
Silicon
Thermal treatment
Cooling rate
Tenso-thermo-emf
Anisotropy parameter of thermo-emf

ABSTRACT

The influence of the annealing temperatures and cooling rates of n-silicon crystals, grown by the Czochralski method and doped with phosphorus impurity, on their electric and thermoelectric properties was studied. In the region of predominantly impurity scattering a more essential dependence of the charge carrier mobility on the cooling conditions of crystals was established in comparison with the dependence on the annealing temperature. The analysis of the measurement results of tensoresistance and tenso-thermo-emf was carried out, on the basis of which the dependence of the anisotropy parameter of drag thermo-emf on the cooling rate was obtained. The feature of the anisotropy parameter of thermo-emf M in the form of its maximal deviation from the linear dependence $M = M(\lg(\upsilon_{cl}))$ was revealed in the region of cooling rates from 8 to 15 K/min.

1. Introduction

Monocrystalline silicon belongs to the strategically important semiconductor materials, which are widely used in micro- and nanoelectronics and significantly change one's physical characteristics under the influence of different physical impacts [1–3]. Devices made on its basis are successfully used both in scientific laboratories and in the industry, including under the influence of radiation, thermal, deformation and other physical fields and their combinations [4–7]. The action of such fields is usually accompanied by a change in the electrophysical properties of silicon, which in turn are often associated with the appearance of new defect states or transformation of existing with the formation of complicated impurity-defective complexes [8].

The rapid progress in the manufacture of semiconductor devices observed in the past few decades, demands the development and creation of new highly efficient materials with predefined characteristics and improved functionality [9,10]. The technologies of manufacturing of the modern semiconductor devices puts ever higher demands to the spatial homogeneity of the parameters of basic material, which stimulates the investigations of kinetic effects in the real crystals [11,12]. The increase in the requirements to the quality of silicon crystals is associated not only with the growing pace of automatization of the industrial and domestic spheres, but also due to the appearance and significant improvement in the field of semiconductor technique of charge-coupled devices for various purposes, ultrahigh-speed very large-scale integrations, super high-power high-voltage thyristors, optical elements of infrared technique, nanotransistors with high-conductivity channels, etc. All this predetermines the need to search of the new technological processes for obtaining the high-quality silicon crystals [13,14].

The thermal treatment in various conditions of solid-state electronic devices with distributed parameters based on silicon crystals is an integral part of the technology of their manufacture [15–17]. The production of modern semiconductor devices is associated with the need to use high-temperature annealings of plates, on the basis of which these devices are created [18]. These annealings are carried out during the oxidation of semiconductor wafers under the photolithography, under the diffusion of doping atoms and other technological operations at the temperatures reaching 1473 K for the several tens of minutes and even several hours. Such annealings of a semiconductor material, on the basis of which the device is made, strongly affect on its electrophysical parameters in comparison with the initial material.

The interaction of dopants with lattice defects and residual impurities in the bulk of semiconductor crystals occurs, in general, is faster at higher temperatures and more slowly at lower temperatures. Since at high temperatures simultaneously with the formation of complexes, their decay also occurs, the cooling rate of the crystals (along with the temperature and time of their annealing) can have significantly effect on the electrophysical properties of silicon crystals [19].

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https://doi.org/10.1016/j.physb.2018.03.021
Received 11 February 2018; Received in revised form 10 March 2018; Accepted 12 March 2018

Table 1
Parameters of the initial and thermally treated n-Si⟨P⟩ crystals.

Thermal treatment conditions		77 K			300 K		
T_{ann}, K; t, h	$\upsilon_{cl,}$ K/min	ρ, Ohm cm	n_e, 10^{-15} cm^{-3}	μ, cm^2/V s	ρ, Ohm cm	n_e, 10^{-16} cm^{-3}	μ, cm^2/V s
1473;2	1000	0.175	4.98	7170	0.318	1.56	1260
	30	0.173	4.92	7340	0.320	1.53	1280
	15	0.170	5.00	7350	0.312	1.54	1300
	1	0.170	4.84	7540	0.314	1.54	1290
773;2	1000	0.183	4.86	7020	0.341	1.49	1230
	30	0.175	5.00	7140	0.319	1.53	1280
	15	0.177	4.88	7230	0.311	1.55	1300
	1	0.168	4.96	7500	0.331	1.48	1270
Initial crystal		0.173	4.77	7590	0.334	1.47	1270

The aim of the paper was to establish the regularities of the influence of thermal annealing and different cooling rates on the change of electric and thermoelectric properties of silicon crystals with a significant concentration of phosphorus impurity.

2. Results and discussion

The experiments were carried out on the silicon crystals (n-Si⟨P⟩) with resistivity $\rho_{300\text{K}} \approx 0.33$ Ohm · cm grown in the [001] direction in the nitrogen atmosphere using the Czochralski method. A high-temperature (at $T_{ann} = 1473$ K with a duration of $t = 2$ h) and a low-temperature (T_{ann}= 773 K; t= 2 h) annealings were used in the work. The crystals were cooled from the annealing temperature to room temperature with the different rates υ_{cl}, K/min: 1000 (fast cooling), 30, 15, 8, 3 and 1 (slow cooling).

The main parameters of the initial and thermally treated crystals are presented in Table 1. It can be seen from Table 1 that both after the high-temperature and after the low-temperature treatment of the crystals (at all the cooling rates studied) the values of resistivity (ρ) and the concentration of charge carriers (n_e) are sufficiently close to the initial data. The insignificant differences in the charge carrier mobility $\mu^{cl}_{77\text{K}}$ and $\mu^{initial}_{77\text{K}}$, which fit into a certain regularity ($\mu^{cl}_{77\text{K}} < \mu^{initial}_{77\text{K}}$), are characteristic for the heat-treated crystals. However, when the cooling rate decreases, these differences are levelled in both cases (at high- and low-temperature treatment). The absence of depletion of the impurity centers at 77 K, that can be described by the expression of $n_{e300\text{K}} \approx 3n_{e77\text{K}}$, is a consequence of the sufficiently high doping level of the investigated n-Si⟨P⟩ ($N_p \approx 1.5 \times 10^{16}$ cm^{-3}), and is observed (see Table 1) both for initial and for thermally treated crystals.

The influence of different thermal treatment regimes on the charge carrier mobility was investigated in the temperature interval, which overlapped (at the specified doping level of the crystal) the region from the predominantly impurity scattering to the predominantly phonon scattering (from 20 to 300 K). The electrical conduction and Hall effect measurements were made on the crystals in the initial state, as well as after high- and low-temperature annealings (with corresponding cooling rates). The dependences of the charge carrier mobility on the temperature $\mu = f(T)$ calculated from the data of Hall measurements for all these cases are represented by the corresponding curves in Fig. 1a (for crystals annealed at 1473 K) and in Fig. 1b (for crystals annealed at 773 K).

The obtained results showed that the charge carrier mobility, measured in the region of predominantly impurity scattering (i.e., at low temperatures 20–50 K), exhibits the marked sensitivity to the conditions of the thermal treatment of n-Si⟨P⟩ crystals. Meanwhile both high-temperature (1473 K) and low-temperature (773 K) annealings lead only to decrease of the charge carrier mobility in this region (see Fig. 1a and b). However, it has been found that the effectiveness of the decrease in mobility depends not so much on the annealing temperature (1473 or 773 K) as on the cooling rate (from T_{ann} to room temperature).

It should be noted that under measuring dependences $\mu = f(T)$ only for high-temperature annealing of the crystals (i.e., when the cooling occurred from 1473 K) the changes of carrier mobility on the cooling rate were observed (Fig. 1a). During the annealing at 773 K, the results of the decrease in mobility (in the temperature region of 20–50 K) practically (within the taking into account the limits of the accuracy of measurements of the Hall coefficient R and resistivity ρ, which are required for the obtaining of μ) did not depend on the cooling rates of the crystals (Fig. 1b).

At high-temperature annealing ($T_{ann} = 1473$ K) Fig. 1a shown that annihilation (or annealing) of primary defects, which lead to the decrease in the mobility values in the impurity scattering region, is

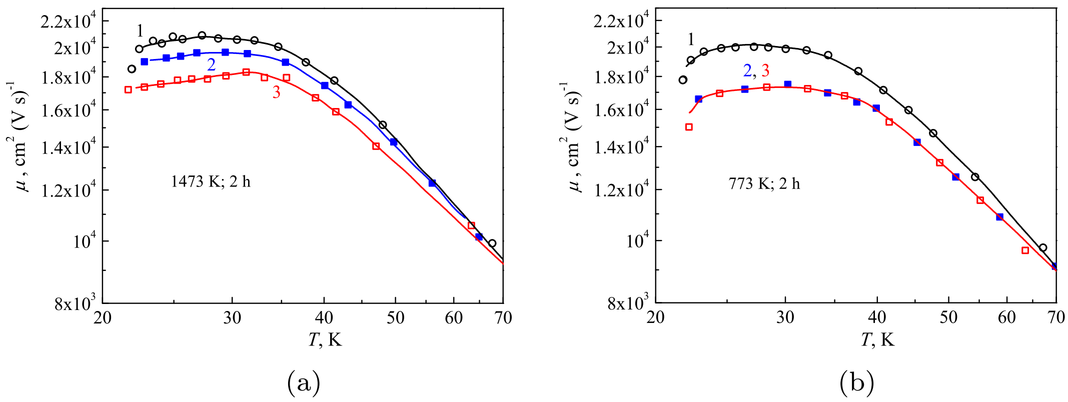

Fig. 1. Temperature dependences of the charge carrier mobility $\mu = f(T)$ for samples of n-Si⟨P⟩ ($n_{e300\text{K}} = 1.47 \times 10^{16}$ cm^{-3}): 1 – in the initial state; after annealing at (a) 1473 K, (b) 773 K and subsequent cooling: 2 – slow (1 K/min); 3 – fast (1000 K/min).