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A Content-Addressable Memory structure using quantum cells in nanotechnology with energy dissipation analysis

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ABSTRACT

Quantum-dot cellular automata is one of the recent new technologies at the nanoscale that can be a suitable replacement for CMOS technology. The circuits constructed in QCA technology have desirable features such as low power consumption, high speed and small size. These features can be more distinct in memory structures. In this paper, we design a new structure for content addressable memory cell in QCA. For this purpose, first, a unique gate is introduced for mask operation in QCA and then this gate is used to improve the performance of CAM. These structures are evaluated with QCADesigner simulator.

1. Introduction

Implemented circuits in CMOS technology have disadvantages such as high power consumption, large physical size and high leakage current [1]. Researchers are looking for new technology to overcome these disadvantages. QCA is one of these technologies [1–3]. QCA is one of the recent new technologies in the nano-scale that can cover flaws in CMOS technology. QCA is a good alternative for circuit design, because the ability to achieve high performance with minimum energy consumption [4,5]. QCA is based on the principle of arrest and repulsive of electrons. The main component of the QCA is the square cell that contains four holes and two electrons. Coulomb repulsion causes the electrons occupied the holes diagonally to each other [4].

Designing an efficient QCA memory cell is a problem that has attracted the attention of scientists. The works such as [6,7] have focused on this problem. These works have presented a Random Access Memory (RAM) cell in QCA. In this paper, we propose a Content-Addressable Memory (CAM) cell, which is different from RAM. CAM is a special type of computer memory that can be used in certain very high speed searching applications. In this type of memory, the time to reach an item stored in memory is significantly reduced [4].

We present a unique structure that can improve the performance of the CAM memory. A two-input XOR gate and a three-input majority gate are used to design the unique structure. Finally, we use QCADesigner simulator to evaluate the performance of the proposed CAM cell.

The rest of this paper is as follows: Section 2 will review the QCA and CAM memory. In Section 3, the proposed unique gate and proposed CAM cell will be introduced. The simulation results based on QCADesigner is provided in Section 4. Conclusion is discussed at the end.

2. Background

In this section, an overview of the QCA and CAM memory is presented.

2.1. QCA

QCA is one of the newest technologies in nanometer dimensions [5]. This technology is based on the cell and provides a new method to design the digital circuits. The performance of the cells in QCA is based on the placement of electrons. A square-shaped QCA cell consists of four quantum dots and two free electrons [3,4]. The movement of electrons in these cells is due to Coulomb force. The placement of electrons in the dots causes logical values of 0 and 1 [20–22]. The structure of QCA cell is shown in Fig. 1.

2.1.1. Basic logical gates

The three-input majority gate and inverter are the basic logical gates in QCA that are shown in Fig. 2 [1,4]. Three-input majority gates has three inputs A, B and C, and one output Maj. The operation of this gate is $M(A,B,C) = AB + AC + BC$. Truth table of this gate is illustrated in Table 1. The two-input AND and OR gates are made by the three-input majority gate. By fixing the value of one of the inputs to −1 and +1 in three-input majority gate, AND and OR gates are constructed.

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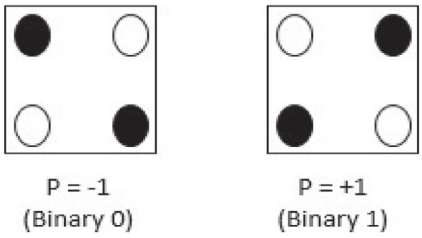

Fig. 1. QCA cell.

2.1.2. Clocking in QCA

A clocking scheme is required in order to control the flow of information in complex circuits [4]. One of the standard and commonly used clocking schemes in QCA is the four-zone scheme [12–19]. The cells can place into different zones. The energy of a clock zone can cause the polarization of the cells in that clock zone. This clocking scheme is shown in Fig. 3.

2.1.3. XOR gate

Another gate that is used in QCA designs is the two-input XOR gate. Various designs have been introduced for two-input XOR gates in QCA [8–11]. The best scheme among these designs is the structure of Fig. 4, which is presented by Ref. [11].

2.2. CAM

A CAM is structure that is purpose-built for extremely fast memory lookups. CAM is capable of searching its entire contents in a single clock cycle. Data stored on CAM can be accessed by searching for the content itself, and the memory produces the match signal and retrieves addresses where that content can be found.

3. The proposed structure

In this section, we propose a new structure to implement a CAM cell.

3.1. The proposed unique gate

In this section, we introduce a proposed unique gate. As previously mentioned, memory design with lower cell count and high speed is one of the most important challenges for researchers. This paper attempts to introduce a unique gate structure that can improve CAM memory performance. The function of this gate is as Eq. (1). To design this gate, an XOR gate introduced in the previous section and a three-input majority gate are used.

$$\text{Out} = \overline{K}(A \odot F) + K \quad (1)$$

The desired operation of this gate is shown in Table 2. If K is "0", the inputs A and F are compared. If k is "1", input values A and F are considered don't care. After checking the function, the design of unique gate in QCA is illustrated in Fig. 5.

3.2. The proposed CAM cell

The QCA layout of the proposed CAM memory cell is shown in Fig. 6. This design is composed of 3 three-input majority gate and 1 proposed

Table 1
Truth table of majority gate.

A	B	C	M (A,B,C)
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

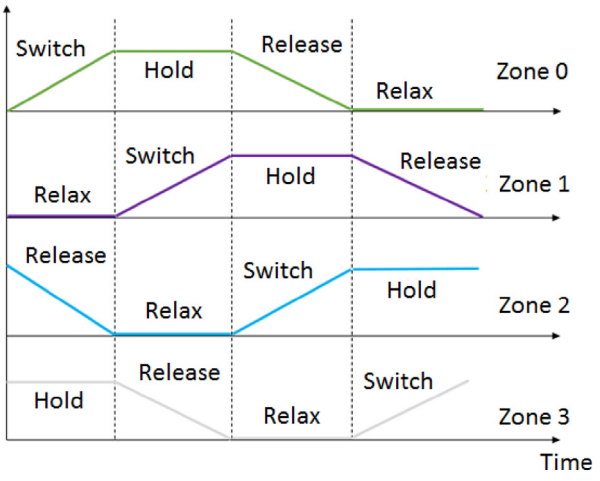

Fig. 3. Clocking scheme in QCA.

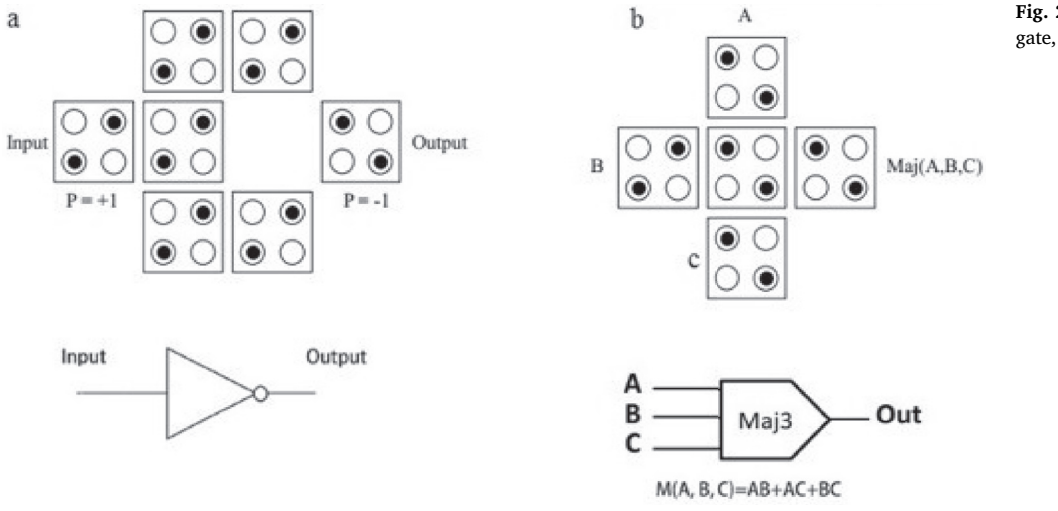

Fig. 2. Basic structures of QCA; (a) inverter gate, (b) three-input majority gate.