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ORIGINAL ARTICLE

Selection of DC voltage magnitude using Fibonacci series for new hybrid asymmetrical multilevel inverter with minimum PIV

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KEYWORDS

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Abstract Multilevel inverters are suggested to obtain high quality output voltage. In this paper, a new hybrid configuration is proposed, obtained by cascading one four switches H-bridge cell with a family of multilevel inverters. In addition, by the use of specific sequence for value of DC sources named Fibonacci series, asymmetrical topology of proposed inverter is introduced. Main advantages are that proposed inverter has least Peak Inverse Voltage (PIV) than other conventional multilevel converters in both symmetric and asymmetric modes. Also, this topology doubles the number of output levels using only one cascaded four switches H-bridge cell. The PCI-1716 DAQ using PC has been used to generate switching pulses in experimental results. For presenting valid performance of proposed configuration, simulation results carried out by MATLAB/SIMULINK software and the validity of the proposed multilevel inverter is verified by experimental results.

1. Introduction

High-power industrial applications of converters have been revolutionized in the recent decades by the advent of multilevel converters [1]. Lately, multilevel converters have presented an important development to reach higher power with increasing voltage levels [2]. Also many multilevel inverter configurations and pulse width modulation (PWM) techniques are presented to improve the output voltage harmonic spectrum [3–5]. Multilevel inverters can be considered as voltage synthesizers, wherein the output voltage is synthesized from many discrete smaller voltage levels. Compared with the traditional two-level voltage inverter, the main advantages of the multilevel inverters are having smaller output voltage step, lower harmonic components, better electromagnetic compatibility and lower switching losses [2,6–9]. They can also operate at both fundamental switching frequency and higher switching frequencies in accord with the implementations [9]. But, the main drawbacks of the multilevel inverters are the use of a larger number of semiconductors and a complex control circuitry and needing the balancing of the voltage at the boundaries of capacitors [10,11].

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From among voltage source multilevel converters, cascaded and modular multilevel converters offer several benefits such as possibility of eliminating ac side filters and interfacing transformer in some applications where it is appropriate, low dv/dt and switching losses as converter switches operate at low frequency [12,13].

In the present paper, a new hybrid symmetric and hybrid asymmetric topology of multilevel inverter has been investigated. In symmetrical mode the value of PIV and the number of switches versus other conventional symmetric converters has been reduced. For magnitude selection of DC voltage sources in asymmetrical mode Fibonacci series [14], has been used. This cause significant reduction in total switches PIV with respect to other multilevel topologies. Simulation results and comparison studies and experimental results verify validity of theoretical consideration.

2. Case study

2.1. Conventional cascaded H-bridge multilevel inverter

One of the basic structures for multilevel inverters is cascaded H-bridge inverter. Fig. 1 shows a single phase cascaded multilevel inverter.

In cascaded H-bridge multilevel inverters each DC source is connected to different stages. If all DC voltage sources in Fig. 1, equal to $V_{dc} = 1pu$, the converter is known as symmetric multilevel inverter. In symmetric topology, each cell can generate three voltage levels $+V_{dc}$, 0, $-V_{dc}$. The number of output voltage levels can be obtained by:

$$m = 2n + 1 \tag{1}$$

and PIV is given by:

$$PIV = 4nV_{dc} \tag{2}$$

where n is the number of DC sources and m is the number of voltage levels. To obtain large number of output voltage levels, asymmetric multilevel inverter can be used. In binary topology of asymmetric cascaded multilevel inverter, maximum output voltage levels and PIV are given by:

$$m = 2^{n+1} - 1 \quad \text{if} \quad V_{dci} = 2^{i-1}V_{dc} \quad \text{for} \quad i = 1, 2, \ldots, n \tag{3}$$

$$PIV = 4(2^n - 1)V_{dc} \tag{4}$$

and in trinary topology, maximum output voltage levels and PIV are given by:

$$m = 3^n \quad \text{if} \quad V_{dci} = 3^{i-1}V_{dc} \quad \text{for} \quad i = 1, 2, \ldots, n \tag{5}$$

$$PIV = 2(3^n - 1)V_{dc} \tag{6}$$

2.2. A symmetrical topology of multilevel inverter

In [15], a new symmetrical topology of multilevel inverter is introduced, as presented in Fig. 2. In this configuration all of negative and positive levels can be obtained.

This configuration consists of DC voltage sources and $(2n + 2)$ unidirectional switches. Maximum output voltage can be obtained as follows:

$$V_{O_{max}} = V_1 + V_2 + \ldots + V_n, \qquad V_1 = V_2 = \ldots = V_n \tag{7}$$

For $V_n = V_{dc}$, maximum output voltage will be $V_{O_{max}} = nV_{dc}$. The number of output voltage levels and PIV can be obtained by:

$$m = 2n + 1 \tag{8}$$

$$PIV = 4nV_{dc} \tag{9}$$

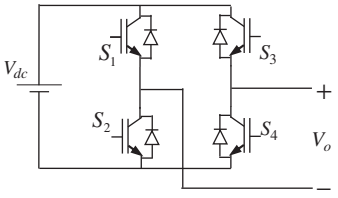

Figure 3 Four switches three level H-bridge inverter.

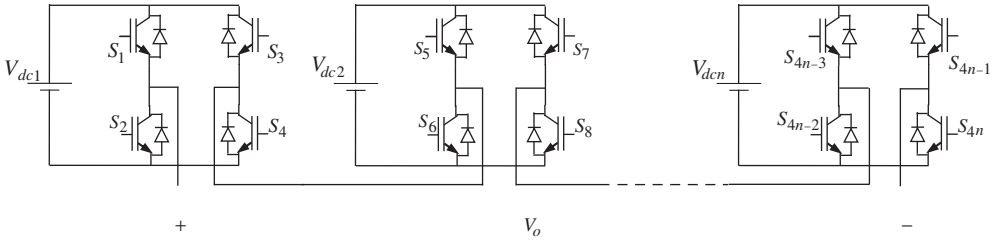

Figure 1 Single phase cascaded multilevel inverter.

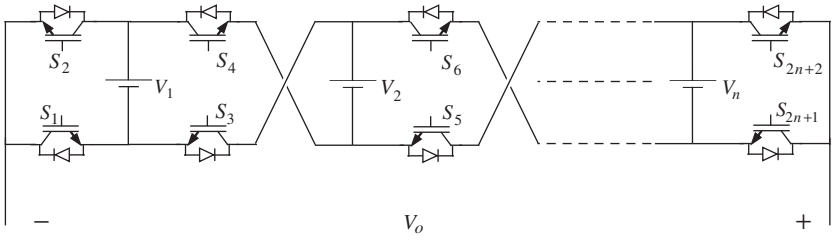

Figure 2 Family of multilevel inverters proposed in [15].