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Capacitance–conductance spectroscopic investigation of interfacial oxide layer in Ni/4H–SiC (0 0 0 1) Schottky diode

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ABSTRACT

In this reported work the interface properties of a process-induced thin interfacial oxide layer present between Ni and 4H–SiC substrate was examined systematically for fabricated Ni/4H–SiC (0 0 0 1) Schottky barrier diodes. Moreover, their contribution in the form of interface traps level density was investigated employing capacitance–conductance (C–C) spectroscopy techniques. The distinctive parameters of interface at Ni and 4H–SiC substrate were determined from the C–C spectroscopy under forward bias condition. The increase in capacitance value towards lower frequencies results from the presence of interface traps at the Ni/4H–SiC interface however the observed maximums peaks in the normalized conductance curve of the diode indicates the presence of an interfacial layer in the fabricated Schottky barrier diode. It has been found that the density of interface traps level decreases (1.25×10^{13}–1.16×10^{13} cm^{-2} eV^{-1}) and time constant of interface traps (3.16×10^{-5}–1.47×10^{-3} s) increases with bias voltage at anode in the range of Ec-0.06 to Ec-1.06 eV from the top of conduction band toward midgap of n-type 4H–SiC substrate. Furthermore, the capture cross section was found to vary from 9.31×10^{-10} cm^2 in (E_c-0.06) eV to 4.43×10^{-11} cm^2 in (E_c-1.06) eV.

1. Introduction

Schottky barrier diode is one of the most fundamental devices in the area of semiconductor device technology. In the current research, the formation of potential barrier with reasonable interface states at metal–silicon carbide (M–SiC) contact is of prime interest [1–5]. The interface states due to the presence of interfacial oxide play a critical role on device characteristics [6]. These interface states control the location on Fermi level in the band gap of SiC and thereby, influence the device parameters significantly. Any process induced mechanism may also affect performance of the Schottky barrier diodes. The presence of thin native oxide at the interface of metal semiconductor contact may be one of the most fundamental mechanisms, which may result in variation of various device parameters from their desired value. The structural change due to the existence of interfacial oxide layer between metal and SiC in Schottky diode forms metal-oxide–silicon carbide (MOSiC) type structure, which stores the electric charge by virtue of the dielectric property of oxide layer. Due to the presence of carbon component [7,8] in the interfacial oxide, which arises during fabrication of silicon carbide (SiC) Schottky structure, the analysis of interface properties is comparatively more complicated than other semiconductor devices [9,10].

SiC based device technology has additional advantage over silicon in the field of semiconductor and electronics. For many decades from the latter half of the twentieth century, SiC is being widely used in various sectors and in several applications where advanced properties of this material such as inherent radiation-resistance, high temperature operating capacity, high voltage and power handling capacity are very much useful for innovative semiconductor device technology. Since then, extensive research studies took place to utilize the unique properties for the development of semiconductor devices and electronic system. Hexagonal SiC polytypes are commonly used in the fabrication of devices particularly Schottky diodes. Several studies have been carried out in the last decade with reference to the electron mobility for 6H–SiC, 4H–SiC and 3C–SiC [11,12]. 4H–SiC shows a two times higher electron mobility than 6H–SiC for low and medium doped layers. Hence, the 4H–SiC polytype is much more attractive to attain the low resistivity layers, which is suitable for vertical power devices. Moreover, the easy formation of thermal oxide layer on SiC surface places this material at top among the different materials in compound semiconductor family.

The interface state density (N_{ss}) and series resistance (R_s) of M–SiC contact in Schottky structures are important parameters that affect their expected electrical parameters [13,14]. When a bias voltage is applied across the diode, the combination of series

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resistance, interfacial oxide layer and depletion layer of device will share the applied voltage and hence the effective applied voltage reduces. There are numerous experimental methods, which could help to determine the N_{ss}, and among them the more important are the conductance techniques developed by Nicollian and Goetzberger [15] for metal oxide semiconductor (MOS) structure on silicon substrate. In Schottky structure, metal and semiconductor are always in direct contact forever. But, in some areas it may be separated by dielectric process induced layer and there is an incessant distribution of N_{ss} at the interface of semiconductor and the dielectric layer. Recently, the interface state density of the Si based Schottky diodes have been experimentally characterized by Tugluoglu et. al. and Beris employing conductance and capacitance characteristics at various frequencies [16,17]. The forward and reverse bias measurement of conductance and capacitance provides the important information about the energy distribution of N_{ss} of Schottky structure associated with interfacial oxide. At high frequencies the charge-discharge of the interface states cannot follow an a.c. signal, while at low frequencies it can easily follow ac signal. In general, conductance and capacitance plots as a function of applied bias are frequency dependent. Moreover, the presence of interfacial oxide layer between metal and SiC surface may result in deviation of the device characteristics from the ideal behavior. In addition, there may be a capacitance due to interface states in excess to depletion layer capacitance, depending on the relaxation time of the interface states and frequency of a.c. signal. It is therefore important to examine the role of interfacial oxide layer, which plays a critical role on device parameters.

In this paper a capacitance–conductance spectroscopy (C–C spectroscopy) was performed at different frequency. The major goal of this study was to investigate interface state densities, relaxation time and capture cross section of the fabricated Ni/4H–SiC (0 0 0 1) Schottky barrier diodes. Experimental details for the fabrication of Schottky barrier diodes and C–C spectroscopy techniques are given in the next section. The measured electrical characteristics and analyzed device parameters are mentioned in the section thereafter. Finally, the technical discussions are given which is followed by conclusions.

2. Capacitance–conductance (C–C) spectroscopy; theoretical background

The main purpose of this reported work is to describe the relation between the measured capacitance and conductance of the M–SiC interface associated with thin oxide layer in between metal and SiC. Interface traps are one types of defects located at the interface of 4H–SiC and native oxide layer. These interface traps have one or more energy levels within the bandgap of 4H–SiC. Capture or emission phenomenon occurs when interface traps change occupancy due to the intersection with conduction band by capturing or emitting electrons and with valence band by capturing or emitting holes. The interface trap levels are detected through the loss resulting from change in this occupancy, which is governed by change in applied gate bias voltage. A small a.c. voltage applied to the anode of a studied structure causes the band edge to move towards or away from the Fermi level, which, in turn, results in to the phenomenon of capture or emission of trap levels. A three dimensional (3D) pictorial diagram of this mechanism is represented in Fig. 1. At a given frequency, for the positive half cycle of applied gate voltage, the conduction band of 4H–SiC moves toward the Fermi level while for negative half cycles this band (conduction) moves away from the Fermi level. As a result, energy loss happens on both halves of the ac cycle, which is supplied by the signal source. This energy loss may be measured using an equivalent parallel conductance (G_p) in the studied

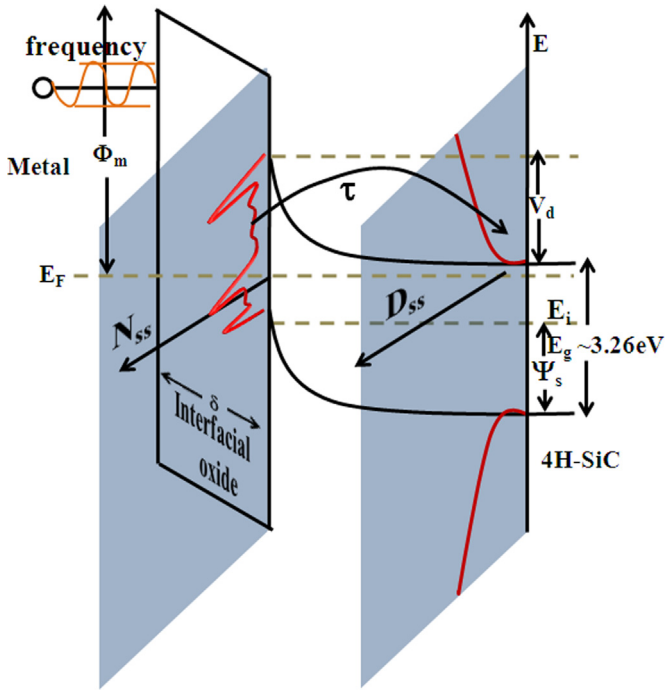

Fig. 1. Schematic representation of energy band diagram of a n-type Ni/4H–SiC structure in which a thin interfacial layer is associated between Ni metal and 4H–SiC substrate. On the application of a dc gate voltage alongwith a ac signal of frequency *f*, causing a band bending Ψs in the 4H–SiC and a interface trap response with time constant.

structure. In addition to an energy loss associated with capture and emission, interface traps also can hold an electron for some time after capture i.e. interface trap store charge. Therefore, there will be a capacitance C_{ss} which is proportional to interface trap level density. At any frequency of ac gate voltage the loss depends on the speed of response of interface traps, determined by either capture probability or the interface trap level density near the Fermi level [18]. For a known value of loss, at various frequencies and bias voltages from experiment, capture cross-section and interface trap level density for energy level within the bandgap of 4H–SiC can be estimated. The interface trap in the studied structures assumes Shockley–Read–Hall (SRH) center located at 4H–SiC and SiO_2 interface.

Interface trap admittance is not measured directly; but it can be extracted from experimentally measured capacitance and conductance of a structure using an equivalent circuit. On the basis of capture and emission of charge carriers by interface trap levels distributed throughout the 4H–SiC bandgap, a general equivalent circuit is derived for the above described structure which is shown in Fig. 2(b) and (c). Employing this circuit, the major parameters governing interface trap capture and emission are extracted from measured capacitance and conductance method. Since, SiC has very low minority carries densities, the conductance method is simplest in depletion region because minority carries effects are not so much significant i.e. in depletion region, interface trap occupancy changes by capture and emission of majority carries (electrons) only. On other hand, capacitance method is simplest in accumulation region, because the drifting of majority carriers can be easily monitored. Using the conductance method, interface traps level density, capture probability and time constant dispersion from the real component of the admittance can be extracted. This method is most precise and sensitive among the small signal steady-state techniques. For these reasons, our present knowledge of the electrical characterization of interface properties is based almost entirely on conductance measurements. On the other hand,