



# Implementation of real-time digital CR–RC<sup>m</sup> shaping filter on FPGA for gamma-ray spectroscopy

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## ARTICLE INFO

### Keywords:

CR–RC<sup>m</sup> shaping  
Gamma-ray spectroscopy  
Semi-Gaussian filter  
Digital signal processing

## ABSTRACT

A novel implementation of a digital CR–RC<sup>m</sup> shaping filter for gamma-ray spectroscopy is presented in this paper, derived from the digitalization and quantization of the input and output voltage of CR and RC circuits. Compared with the conventional digital CR–RC<sup>m</sup> shaper, it has a relatively simple structure consuming fewer multipliers and is easy to realize on DSP chips. More importantly, this digital shaper also overcomes the shortcoming of the conventional digital CR–RC<sup>m</sup> shaper, which lacks the function of pole-zero cancellation (PZC). Experimental data on noise suppression, immunity to ballistic deficit, and energy resolution improvement show that the digital spectroscopy system based on the described shaper achieves the same excellent performance as the analog spectroscopy system from CANBERRA, which therefore provides a new way to realize the shaping of digital signals from radiation detectors, and this carries great significance for engineering applications.

## 1. Introduction

Currently, digital signal processing (DSP) is widely used in gamma spectroscopy systems. A general block diagram of a digital gamma spectroscopy system is shown in Fig. 1 [1]. It consists of two blocks: one is the detector usually integrated with a preamplifier, and the other is composed of an adapter circuit based on an anti-aliasing filter and a single-ended to differential amplifier with adjustable gain, an analog-to-digital converter (ADC), and a DSP chip. In the digital system shown in Fig. 1, the preamplifier's output signals are directly digitized by ADC. In the following, all signal processing operations, including pulse shaping and pile-up processing, are carried out by programmable DSP chips.

Pulse shaping, which is to shape the signal to optimize the spectrometer's performance, such as immunity to ballistic deficit effect, pile-up rejection and signal-to-noise ratio, plays the most important role of all DSP operations [2]. CR–RC<sup>m</sup> shaping is one of the most widely used shaping methods in analog gamma spectroscopy systems. A recursive implementation of a digital Gaussian shaper based on wavelet analysis is proposed in [3,4], but it is too complicated to realize in DSP chips. The real-time digital CR–RC<sup>m</sup> shaping algorithm described in [5] has pretty good logic control and pipelined processing but with the shortcoming of lacking the function of pole-zero cancellation (PZC) and of its notable complexity for implementation on an FPGA chip.

Considering the advantages of FPGA, a novel implementation of a digital CR–RC<sup>m</sup> shaper is proposed. Based on research work to improve the shaper's performance in noise suppression, immunity to

ballistic deficit, and pile-up rejection through simulations, an optimized digital spectroscopy system is implemented. In the meantime, many experiments are conducted for this digital system to obtain performance data on the shaper's energy resolution improvement and additionally to explore the performance difference between the presented system and the conventional analog spectroscopy system from CANBERRA.

The rest of the paper is organized as follows. A review of analog CR–RC<sup>m</sup> shapers is described in Section 2. In Section 3 and Section 5, the novel digital CR–RC<sup>m</sup> shaper and its implementing strategies for FPGA are presented. Then, Sections 4 and 6 outline the simulation and experimental results of the shaper's performance. Finally, the conclusion is drawn in Section 7.

## 2. CR–RC<sup>m</sup> shaper

As shown in Fig. 2, analog CR–RC<sup>m</sup> shaping filter is a network of one CR differentiator followed by m RC integrators with a suitable cascade arrangement. The number of RC integrators is the order number of the shaper.

From [2], the transfer function of the CR–RC<sup>m</sup> shaping filter in the Laplace domain can be easily obtained as (1).

$$H(s) = \frac{s \cdot RC}{(1 + s \cdot RC)^{n+1}} \quad (1)$$

With bilinear transformation in [6], the transfer function of the CR–RC<sup>m</sup> shaper in the discrete-time domain could be obtained as (2)

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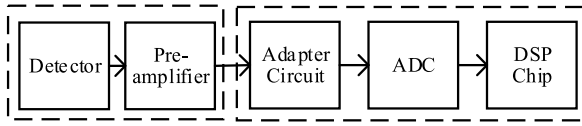


Fig. 1. Typical block diagram of digital gamma spectroscopy system.

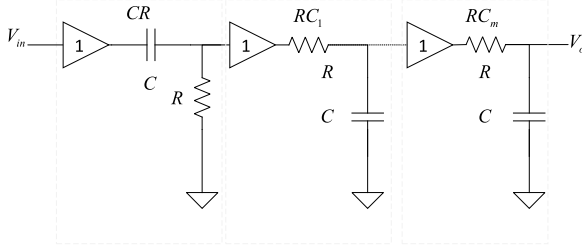


Fig. 2. Schematic of CR-RC<sup>m</sup> filter.

Table 1

Algorithm details obtained through the bilinear transformation of CR-RC<sup>m</sup> filters for order 1–4.

$m$	Algorithm details
1	$V_o[n] = \frac{V_{in}[n]}{P_1^2} - \frac{V_{in}[n-2]}{P_1^2} - \frac{2P_2 \cdot V_{in}[n-1]}{P_1} - \frac{P_2^2 \cdot V_{in}[n-2]}{P_1^2}$
2	$V_o[n] = \frac{V_{in}[n]}{P_1^3} + \frac{V_{in}[n-1]}{P_1^3} - \frac{V_{in}[n-2]}{P_1^3} - \frac{V_{in}[n-3]}{P_1^3} - \frac{3P_2 \cdot V_{in}[n-1]}{P_1} - \frac{3P_2^2 \cdot V_{in}[n-2]}{P_1^2} - \frac{P_2^3 \cdot V_{in}[n-3]}{P_1^3}$
3	$V_o[n] = \frac{V_{in}[n]}{P_1^4} + \frac{2 \cdot V_{in}[n-1]}{P_1^4} - \frac{2 \cdot V_{in}[n-3]}{P_1^4} - \frac{V_{in}[n-4]}{P_1^4} - \frac{4P_2 \cdot V_{in}[n-1]}{P_1} - \frac{6P_2^2 \cdot V_{in}[n-2]}{P_1^2} - \frac{4P_2^3 \cdot V_{in}[n-3]}{P_1^3} - \frac{P_2^4 \cdot V_{in}[n-4]}{P_1^4}$
4	$V_o[n] = \frac{V_{in}[n]}{P_1^5} + \frac{3 \cdot V_{in}[n-1]}{P_1^5} + \frac{2 \cdot V_{in}[n-2]}{P_1^5} - \frac{2 \cdot V_{in}[n-3]}{P_1^5} - \frac{3 \cdot V_{in}[n-4]}{P_1^5} - \frac{V_{in}[n-5]}{P_1^5} - \frac{5P_2 \cdot V_{in}[n-1]}{P_1} - \frac{10P_2^2 \cdot V_{in}[n-2]}{P_1^2} - \frac{10P_2^3 \cdot V_{in}[n-3]}{P_1^3} - \frac{5P_2^4 \cdot V_{in}[n-4]}{P_1^4} - \frac{P_2^5 \cdot V_{in}[n-5]}{P_1^5}$

Here,  $P_1 = (T + 2RC)/2RC$ ,  $P_2 = (T - 2RC)/2RC$ .

through (1).

$$H(z) = \frac{\frac{2RC}{T} \cdot (1 - z^{-1}) \cdot (1 + z^{-1})^m}{\left( \left(1 + \frac{2RC}{T}\right) + \left(1 - \frac{2RC}{T}\right) \cdot z^{-1} \right)^{m+1}} \quad (2)$$

where  $T$  is the sampling period of ADC.

Detailed algorithms, as shown in Table 1, of the digital CR-RC<sup>m</sup> shaper can be obtained through (2).

However, the transfer function (2) is too complicated to realize on DSP chips, especially on FPGA chips.

It is noteworthy that the shaper exhibited in Fig. 2 does not have the function of PZC. If taking the PZC into account, the transfer function will be more complicated than in (2). To solve this problem, an optimized digitalization implementation is introduced in detail in the next section.

### 3. CR-RC<sup>m</sup> shaper's digitalization

As is commonly known, it is too complicated to digitize the CR-RC<sup>m</sup> filter directly. To deal with this challenge, the divide-and-conquer strategy is applied by dividing the digitalization process into three simple procedures: (a) decomposing the shaper into one CR differentiator and  $m$  RC integrators; (b) digitizing the CR differentiator and the RC integrator separately; (c) reconstructing the CR-RC<sup>m</sup> filter with a digitalized CR differentiator and RC integrator.

#### 3.1. Digitalization of CR and RC filter

From the circuit depicted in Fig. 3(a), the input voltage  $V_{in}$  and output voltage  $V_o$  of CR differentiator is related by the following

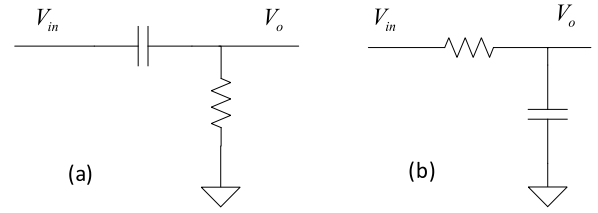


Fig. 3. Schematic of CR and RC circuit.

equation:

$$RC \cdot \frac{dV_o(t)}{dt} + V_o(t) = RC \cdot \frac{dV_{in}(t)}{dt} \quad (3)$$

In consideration of the digital signal  $V_{in}[n]$  and  $V_o[n]$ , the discrete digital signal sequences obtained by the ADC real-time sample and quantize  $V_{in}(t)$  and  $V_o(t)$  (3) can be written as follows:

$$\frac{V_o[n] - V_o[n-1]}{T} + \frac{V_o[n]}{RC} = \frac{V_{in}[n] - V_{in}[n-1]}{T} \quad (4)$$

where  $T$  is the sampling period of ADC. By applying  $d = RC/(RC + T)$ , (4) can be simplified into the following form as:

$$V_o[n] = d \cdot (V_{in}[n] - V_{in}[n-1]) + d \cdot V_o[n-1] \quad (5)$$

It can be easily determined from (5) that the digital CR differentiator is a recursive digital filter.

Similarly, the relationship of analog input voltage  $V_{in}$  and output voltage  $V_o$  of the RC integrator, as shown in Fig. 3(b), satisfies the following formula:

$$RC \cdot \frac{dV_o(t)}{dt} + V_o(t) = V_{in}(t) \quad (6)$$

The relationship of the digital RC integrator's input and output signals also can be obtained as follows:

$$V_o[n] = (1 - d) \cdot V_{in}[n] + d \cdot V_o[n-1] \quad (7)$$

where  $d = RC/(RC + T)$  and  $T$  is the sampling period of ADC.

#### 3.2. Transfer function and frequency response of the CR and RC filter

It is necessary to obtain the transfer function of digital CR and RC filters to create the realization block diagram and illustrate their frequency response.

The transfer function of the digital CR filter can be deduced from (5) with the standard approach in [7] by taking z-transforms of both sides for (5) and solving the ratio.

$$V_o(z) = d \cdot V_{in}(z) \cdot (1 - z^{-1}) + d \cdot V_o(z) \cdot z^{-1} \quad (8)$$

$$H_{CR}(z) = \frac{V_o(z)}{V_{in}(z)} = \frac{d \cdot (1 - z^{-1})}{1 - d \cdot z^{-1}} \quad (9)$$

Clearly, (9) is the transfer function of the digital CR filter. Thus, similarly we can obtain the transfer function of the digital RC filter as (11) from (7) in the same way.

$$V_o(z) = V_{in}(z) \cdot (1 - d) + d \cdot V_o(z) \cdot z^{-1} \quad (10)$$

$$H_{RC}(z) = \frac{V_o(z)}{V_{in}(z)} = \frac{1 - d}{1 - d \cdot z^{-1}} \quad (11)$$

The frequency response of the digital CR and RC filter can be deduced by replacing  $z$  with  $e^{j\omega}$ —a method to obtain the frequency response in [7]—in  $H_{CR}(z)$  and  $H_{RC}(z)$ .

$$H_{CR}(e^{j\omega}) = \frac{d \cdot (1 - e^{-j\omega})}{1 - d \cdot e^{-j\omega}} \quad (12)$$

$$H_{RC}(e^{j\omega}) = \frac{1 - d}{1 - d \cdot e^{-j\omega}} \quad (13)$$

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