Nuclear Inst. and Methods in Physics Research, A 904 (2018) 171–178

Contents lists available at ScienceDirect

Nuclear Inst. and Methods in Physics Research, A

journal homepage: www.elsevier.com/locate/nima

# Model to predict the number of transistors in an asymmetrical priority Address-Encoder and Reset-Decoder readout circuit for monolithic active pixel sensors for high-energy physics

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ARTICLE INFO

*Keywords:*
Monolithic active pixel sensor
Priority Address-Encoder/Reset-Decoder readout circuit
Arithmetic series
Geometric series
Transistor number prediction

ABSTRACT

The digital circuit layout in the active pixel sensor usually occupies the remaining area of an analog circuit layout. Thus, the number of transistors in the readout circuit is an important factor that enables the size of the implementation area to be predicted, when the digital layout of the readout circuit is placed in the specific area. Therefore, the requirement of reducing implementation area of the monolithic active pixel sensor in high-energy physics experiment make it is important to find the optimal readout circuit structure with minimum number of transistors. This study utilizes arithmetic and geometric series to propose a model to predict the number of transistors based on the Karnaugh map of the priority Address-Encoder and Reset-Decoder readout circuit. The proposed prediction model can list all the probable architectures of the priority Address-Encoder and Reset-Decoder readout circuit. In addition, the model is able to highlight the structure that contains the minimum number of transistors, even when the bit-width of the input states of the basic blocks in every layer are different, instead of calculating the number of transistors based on the assumption that the bit-width of the input states of the basic block in every layer are same, like the traditional prediction model. A comparison of the results obtained with the Cadence post-layout simulation and FPGA implementation shows that the number of transistors calculated by the proposed model is of the same order of magnitude to that obtained from the Cadence post-layout simulation and FPGA implementation.

## 1. Introduction

Monolithic active pixel sensors (MAPSs) have been widely used in high-energy particle physics experiments to detect particle trajectories [1–7]. Compared with other readout architectures [8–10], the priority Address-Encoder and Reset-Decoder (AERD) readout circuit was recently employed in the MAPS chip, because it can reduce the readout time and power consumption [11]. The traditional and symmetrical AERD network architecture to decode 16 pixels is shown in Fig. 1. It can be seen from Fig. 1 that the bit-width of the input states in every basic priority block of different layers are equal to 4, in both the symmetrical and traditional AERD circuits.

According to the published calculation of the minimal implementation area in literature [8], the two main contributors to the area occupied by a digital circuit are the routing channels and the number of transistors. Since the digital circuit layout is usually placed in the remaining area of the analog circuit layout, the AERD circuit layout of an active pixel sensor is located among the layout of pixels in the layout of double columns as shown in Fig. 4 of literature [11], which is a common structure of MAPS employed in high-energy particle physics. On the basis of these published results in literature [8] and literature [11], it can be concluded that the number of transistors has an important impact on the size of the implementation area, when the digital circuit layout is placed in the specific area.

According to the literature [11], when the bit-width of the input states of the basic block in an AERD circuit is 4, as shown in Fig. 1, the number of transistors in an AERD circuit reaches a minimum, accordingly, the implementation area of the AERD circuit is minimized.

However, this conclusion drawn from the literature [11] is made on the assumption that the AERD circuit is symmetrical, namely that the bit-width of the input states of the basic block in every layer are the same. In actual high-energy particle physics experiments, this assumption will reduce the number of the probable AERD network architecture, which will miss the AERD network architecture with minimal number of transistors, especially when the number of input

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https://doi.org/10.1016/j.nima.2018.07.041
Received 18 December 2017; Received in revised form 18 May 2018; Accepted 16 July 2018
Available online 21 July 2018

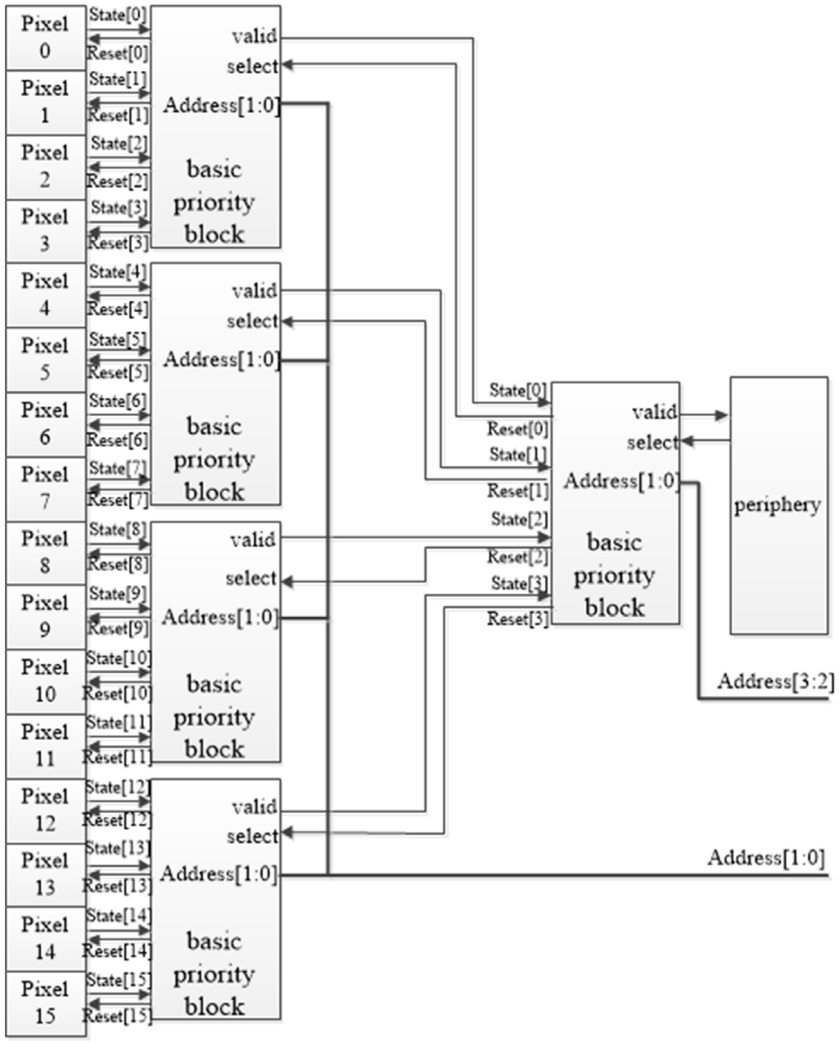


**Fig. 1.** Symmetrical network of the AERD circuit to decode 16 pixels.

pixels is not an integer power of 2. In order to overcome this defect, this paper proposes a model to predict the number of transistors in an asymmetrical priority AERD circuit by employing an arithmetic series, a geometric series, and a Karnaugh map. An asymmetrical priority AERD circuit means that the bit-width of the input states of the basic block in every layer are not the same.

The structure of this paper is as follows: the proposed model to predict the number of transistors is presented in Section 2, the simulation results and their comparison with the layout results are provided in Section 3, and Section 4 concludes the paper.

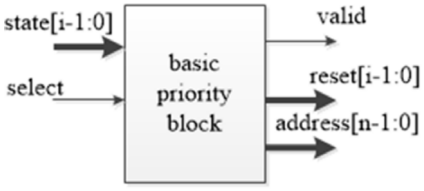


**Fig. 2.** Structure of a basic priority encoder block.

## 2. Proposed model for prediction of number of transistors

The model for predicting the number of transistors in AERD circuit comprises two major parts: predicting the number of transistors in intra-layer and inter-layer circuits, respectively. The intra-layer circuit is the circuit in every layer, while the inter-layer circuit is the circuit between adjacent layers.

### *2.1. Model for predicting the number of transistors in a basic priority encoder block*

Basic priority encoder block is the main component of intra-layer circuit of AERD circuit. In the same layer, the bit-width of the input states of every basic priority encoder block is the same. The structure of a basic priority encoder block is shown in Fig. 2. The definitions of all signals in basic priority encoder block are shown in Table 1.

The relationship between $i$ and $n$ is: $2^n = i$. The structures of standard CMOS gate are shown in Fig. 3.

The output signals of the basic priority encoder block include three parts: valid, reset, and address. Three part of circuits produced by these three output signals and corresponding numbers of transistor are shown as follows:

(1) valid circuit

Because valid = state[0] + state[1] + ⋯state[$i$ − 1], according to the structure of a standard CMOS gate, as shown in Fig. 3, one bit input variable needs a corresponding pair of P-MOS and N-MOS transistors in the NOR logic gate, and there are two transistors in one Inverter logic gate. As a result, the NOR logic gate with $i$ bit input variables needs $2 * i$