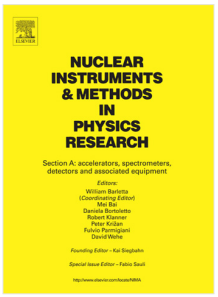
Accepted Manuscript



28 nm Integrated Circuit for PIXel detector

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PII: S0168-9002(18)30597-7
DOI: https://doi.org/10.1016/j.nima.2018.05.012
Reference: NIMA 60796

To appear in: *Nuclear Inst. and Methods in Physics Research, A*

Received date : 5 October 2017
Revised date : 3 May 2018
Accepted date : 6 May 2018

Please cite this article as: F. Resta, A. Pipino, M. De Matteis, A. Baschirotto, 28 nm Integrated Circuit for PIXel detector, *Nuclear Inst. and Methods in Physics Research, A* (2018), https://doi.org/10.1016/j.nima.2018.05.012

28nm Integrated Circuit for PIXel detector

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Abstract

IC-PIX28 (Integrated Circuit for PIXel detectors) is an analog read-out front-end fabricated in 28 nm Bulk-CMOS technology to process the charge signal produced by the pixel detector having 100 fF parasitic capacitance. The device is composed by a Charge Sensitive Pre-amplifier (CSPreamp) and a comparator. The development of IC-PIX28 manages several issues due to the poor analog performance of the standard-process MOS transistors in 28 nm Bulk-CMOS technology, whose choice is motivated by the expected rad-hard performance up to 1 Grad of Total Ionizing Dose. IC-PIX28 achieves performance robustness and low-power consumption by specific circuital solutions and it operates from a single 900 mV supply voltage. The full IC-PIX28 read-out channel consumes 4.3 µW. The CSPreamp performs 35 mV/fC sensitivity, 40 dB Signal-to-Noise Ratio, and 0.033 fC (204 e^-_{rms}) Equivalent Noise Charge. Moreover, a switched-capacitors inverter-based comparator performs the Time-over-Threshold (ToT, at very low power consumption) with a measured ToT range of 500 ns convertible in a digital word with a high bit resolution (> 14).

Keywords: CMOS; Front-End; High-Energy-Physics experiments; Pixel Detector; Scaling-Down.

1. Introduction

Researchers exploit the Large Hadron Collider (LHC) at CERN to study the fundamental constituents of the matter. ATLAS (A Toroidal Lhc ApparatuS) and CMS (Compact Muon Solenoid) are two extremely large experiments used to characterize the physics particles in terms of energy (up to 14 TeV), trajectory, type, etc. To increase the efficiency and the reliability of the data, the experiments employ different topologies of detectors and dedicated read-out front-end (specific details on experiment setup are given in [1] and [2]). The electronics read-out, directly interfaced with the detector, obviously plays a key role in High-Energy-Physics (HEP) experiments.

Beyond 2023, HEP experiments will upgrade and the LHC will be replaced with High Luminosity (HL-) LHC. An increment of luminosity up to 5 x 10^{34} cm^{-2} s^{-1} is expected with joined detector improvements.

In presence of all these changes, electronics will have to guarantee the target signal processing performance even in presence of a particle rate of about 2 GHz/cm^2 and an extremely high Total-Ionizing-Dose (TID) [3]. Up to 1 Grad level of TID must be taken into account for Phase-II LHC Upgrades. Such electronics will be developed for proper silicon pixel sensors (i.e. [4]) searching the most suitable circuit design and/or implementation technique to maximize the performance without neglecting the main role of the selected technological Integrated Circuit (IC) node.

The signal processing performance to be guaranteed includes the capability of detecting and converting a very small charge (few fC) in a very short time (< 25 ns). In a generic high-energy physics electronics system, the analog front-end input charge is produced by elementary particle collisions at a rate of 10 - 100 MHz and every collision generates up to one hundred input charges with few picoseconds of lifetime [5].

A generic CMOS Pixel Sensors (APSs [6][7]) matrix with N rows and M columns is shown in Fig. 1. The read-out front-end channels are close to the sensors with more benefits in terms of compatibility, loss information and reliability. The interaction of one or more ionizing particles with the sensor produces charged

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