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# Design and testing of a bunch-by-bunch beam position transverse feedback processor

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ABSTRACT

Shanghai Synchrotron Radiation Facility (SSRF) is a 3.5 GeV storage ring with a bunch rate of 499.654 MHz, harmonic number of 720, and circumference of 432 meters. SSRF injection works at 3.5 GeV, where the multi-bunch instabilities limit the maximum stored current. In order to suppress multi-bunch instabilities caused by transverse impedance, a bunch-by-bunch transverse feedback system is indispensable for SSRF. The key component of that system is the bunch-by-bunch transverse feedback electronics. An important task in the electronics is precise time synchronization. In this paper, a novel clock synchronization and precise delay adjustment method based on the PLLs and delay lines are proposed. Test results indicate that the ENOB (Effective Number Of Bits) of the analog-to-digital conversion circuit is better than 9 bits in the input signal frequency range from 100 kHz to 700 MHz, and the closed loop attenuation at the critical frequency points is better than 40 dB. The initial commissioning tests with the beam in SSRF are also conducted, and the results are consistent with the expectations.

## 1. Introduction

Shanghai Synchrotron Facility (SSRF) is a 3.5 GeV, 300 mA, the third generation synchrotron light source. It consists of a full energy injector including a 100 MeV linac and a 3.5 GeV booster, a 3.5 GeV storage ring and synchrotron radiation experimental facilities. The specifications of SSRF storage ring [1] are presented in Table 1.

A total of 720 bunches circulate in the tunnel with a duty ratio of 500:220 and a turn-by-turn (TBT) frequency marked as $f_{mc}$ = 693.964 kHz ($1/f_{mc}$ corresponds to the period that a bunch circulates in the storage ring of SSRF). The multi-bunch couple oscillation limits the maximum stored current, and the $f_{mc}$-normalized frequencies of the position oscillation in horizontal direction ($X$ direction) and vertical direction (Y direction) are 22.22 and 11.29, respectively. In order to suppress the instability caused by the transverse impedance, a bunch-by-bunch transverse feedback system is indispensable for SSRF [2]. Many efforts have been devoted to the transverse feedback systems over decades. There are mainly two types of systems: one is the frequency domain feedback system called mode-by-mode transverse feedback system, and the other is the time domain feedback system called bunch-by-bunch feedback system [3]. With the development of the electronics design technology, the bunch-by-bunch transverse feedback system has become more widely used.

As shown in Fig. 1, the transverse feedback system designed for SSRF consists of bunch position monitors (BPMs), a hybrid network, an analog front end, a feedback processor, power amplifiers and kickers. The basic method used in SSRF is the single-loop two dimensional feedback technique [4]. The hybrid network imports the signals from two BPMs. Signals from the two skewed position electrodes in the diagonal positions of the BPM2, marked as P1 and P2 in Fig. 1, are used to generate a difference signal (i.e. P2–P1), which contains the position oscillation information in both $X$ and $Y$ directions; signals are also extracted from the four electrodes of the BPM1 and used to obtain the sum signal of these four inputs, which is a stable signal functioning as the Local Oscillation (LO) signal for the down converter in the analog front end [2]. After down conversation, the oscillation information is converted to a beam position signal in baseband (250 MHz) with a peak-to-peak amplitude value of 2 V. In the feedback signal processor, this beam position signal is digitized bunch by bunch, and feedback signals ($X$ direction and $Y$ direction) are calculated by the FPGA, respectively, in the processor, and finally converted back to analog signals that drive the kickers to damp the bunch instability. The latency of the system

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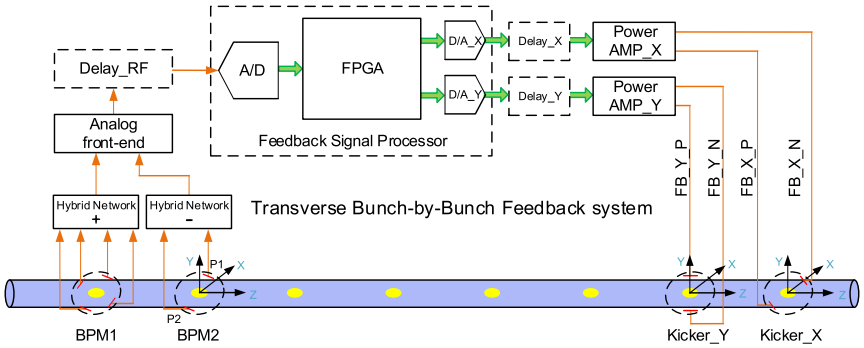


**Fig. 1.** Architecture of the overall beam transverse feedback system.

**Table 1**
Main parameters of the SSRF storage ring.

| | |
|---|---|
| Energy (GeV) | 3.5 |
| Circumference (m) | 432 |
| Harmonic number | 720 |
| Beam current, multi-bunch (mA) | 200–300 |
| Betatron tunes, Qx/Qy | 22.22/11.29 |
| RF frequency (MHz) | 499.654 |

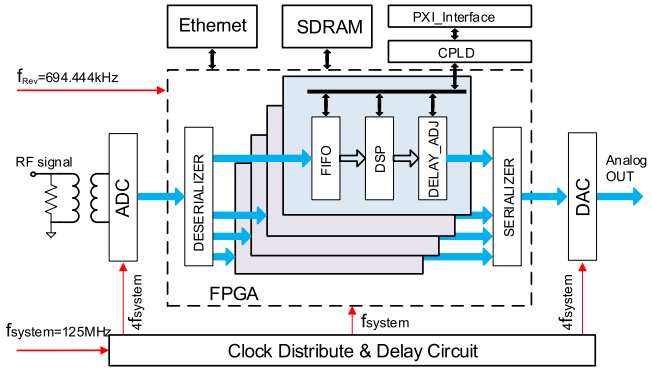


**Fig. 2.** Structure of the beam position transverse feedback processor.

from BPM2 to the kickers (kicker_X and kicker_Y) should be one or two circulation periods of the ring plus bunch propagation delay between the BPM2 and the kickers [5]. In the transverse feedback system at SSRF, the digital signal processing electronics is a key component.

## 2. Digital signal processing electronics design

Aiming at the above application requirement, we designed a beam feedback signal processor, whose structure is shown in Fig. 2, which is based on the PXI (PCI eXtensions for Instrumentation) [6] and integrated into an IPC (Industrial Personal Computer) to guarantee a good stability. The signal from the analog front end is digitized by the Analog-to-Digital Converter (ADC) with a sampling frequency of 500 MHz, which equals to the repetition frequency of a beam bunch in the storage ring, and thus the beam is digitized bunch by bunch. The output of the ADC is then fed to a Field Programmable Gate Array (FPGA) to calculate the feedback response to the position oscillation of each bunch, The feedback information is then converted back to an analog signal by a Digital-to-Analog converter (DAC) in the signal processor, and finally fed to the kickers to suppress the beam position fluctuation. The digital signal processor contains several blocks, which will be discussed in the following sections.

### 2.1. Design of ADC front-end coupling circuits

To make the electronics is sensitive enough to detect and react to the oscillation of every bunch, a 12-bit 500-Msps ADC chip AD9434 is employed in the feedback processor. In the high-speed high-resolution analog-to-digital conversion circuits, the front end coupling circuit is a kernel part in the receiver design, and it is used to implement the single to differential conversion, impedance matching and amplitude adjustment. The purpose of amplitude adjustment is to match the full-scale range of the ADC. As shown in Fig. 3, the cascaded transmission line transformers (ETC1-1-13) are used to provide additional isolation and reduce unbalanced capacitive feedthrough [7]. Using this scheme, a greater bandwidth, lower loss, and better frequency response can be achieved.

To estimate the performance of the circuit, we conducted simulations based on the $S$ parameters. The $S$ parameters of every RF chip are given by the chip manufactures, and they provide the information on how the chip operates at input signal with different frequencies. The $S$ parameters are widely used in the RF circuit design and simulation. The simulation results of the S11 parameter (i.e. reflection ratio) in the frequency range from 100 kHz to 700 MHz are shown in Fig. 4. Shown in Fig. 5 is the amplitude simulation results of the S21, which denotes a forward transmission response of a coupling circuits. Fig. 6 is the phase shift simulation results, in which we can observe that a linear phase response is obtained. In the simulation process, by adjusting the parameters of resistance and capacitance, a balance was achieved between the signal amplitude attenuation and the reflection coefficient caused by the front-end circuits.

### 2.2. Design of clock generation and fine delay adjustment circuits

The feedback system relies on a strict timing [8] (a precision better than 20 ps is preferred for SSRF). First, the sampling clock phase of an ADC needs to be finely adjusted (with a step size of 10 ps) to make the samples at the bunch waveform nearby its peak, in order to improve the Signal to Noise Ratio (SNR). Second, the clock of the DAC also needs to be delayed for a certain time, which make the feedback takes effect at the right time point when the beam bunch passes through the kickers. To meet the above requirements, usually, the cables with different lengths or delay lines are employed to achieve a signal delay in transverse feedback systems in SSRF, NSL2, TLS, PF [2,9–11], as shown in Fig. 1.

The selection of a suitable cable became an inconvenient task. In this paper, a signal delay scheme is proposed based on multiple levels of coarse-time and fine-time adjustments, and it consists of the FPGA logic, multiple stages of the PLL chips and external delay line chips, as shown in Fig. 7. Fig. 8 shows the time relationship of the key clock signals in this processor. The clock circuits consists of the cascaded two delay line chips (DelayLine1 and DelayLine2 in Fig. 7, SY89295 with 10 ps step size) and two PLL chips (PLL1 and PLL2 in Fig. 7, LMK04803). The PLL is featured with a low-noise clock jitter cleaner containing a