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Implementation of the VMM ASIC in the Scalable Readout System

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ABSTRACT

The Scalable Readout System (SRS) developed by the RD51 collaboration is a versatile and multi-purpose approach, which is used with different front-end chips to transfer data from detectors to computers. Targeting mainly micro-pattern gaseous detectors, the system is also applicable for silicon strip or pad detectors. The most frequently used front-end chip today is the APV25, originally developed for the CMS pixel detector. In the scope of the ATLAS New Small Wheel upgrade, a new front-end chip, the VMM, is developed, which has significantly improved specifications compared to the APV25.

We report on the implementation of the VMM in the Scalable Readout System carried out by the RD51 collaboration in the framework of a detector project related to the European Spallation Source ERIC. Due to the hierarchical design of the Scalable Readout System, only specific parts of the readout chain need to be adapted or designed, which is the carrier board for the front-end chip, an adapter card that connects to the common hardware of the system and the firmware for a field programmable gate array. In addition, we have developed dedicated software for slow control, data acquisition and online monitoring. The readout system has been tested in the laboratory and in particle beams and we present results which proof the functioning of the system, even though it is still in a prototype state.

1. Introduction

Most radiation detectors, not only in the field of particle physics, are based on the principle of reading out charge signals. To obtain spatial information about the incident radiation, they include separated detection elements and hence have many readout channels. High density electronics is required in order to process charge signals by amplification, shaping and digitisation. In the field of Micro-Pattern Gaseous Detectors [1] (MPGDs), strip, pixel or pad anodes are used to collect the amplified charge of ionising particles traversing a gas volume. Because of the small size of detector elements, integrated circuits are used and mounted close to the detector to process charge signals. Several Application Specific Integrated Circuits (ASICs) have been designed for different applications. The RD51 collaboration, which facilitates the development of these types of detectors, has developed a multi-purpose readout system, the Scalable Readout System [2] (SRS), in which many different ASICs can be implemented.

Within the BrightnESS project [3] connected to the European Spallation Source ERIC (ESS) [4], one such ASIC, the VMM [5] developed by Brookhaven National Laboratory (BNL), is implemented in the system. The VMM is designed for the ATLAS New Small Wheel project for the upgrade of parts of the muon system, where it is used to read out Micromegas [6] and small-strip Thin Gap Chambers (sTGC) [7].

In our contribution to BrightnESS, the VMM serves as readout for a neutron GEM [8] detector based on a gadolinium converter [9] for the NMX instrument [10]. The SRS readout chain will be capable to cope with the high data rates [11]. Besides of this application, the system is already used for developments in the framework of the ALICE FoCal-E Pad detector [12].

2. The Scalable Readout System

Developed by the RD51 Collaboration since 2009, the SRS features high flexibility, uses commercially available components and presents

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a complete solution for detector readout, starting from minimal table top systems and scaling up to large rack-based systems. In contrast to application specific readout systems, SRS represents a general-purpose approach, consisting of a common back-end and detector specific front-end, which has to be adapted to the specific needs of the experiment it shall be used for. This approach reduces costs and manpower, as only the user-specific part of the system has to be developed for a new application.

A schematic drawing of the complete electronics chain is shown in Fig. 1. It starts at the detector side with the so-called hybrid, a user-specific front-end ASIC on a printed circuit board (PCB) attached to the charge detecting structure of the detector. A number of different front-end ASICs have been implemented in the SRS, for instance the APV25 [13], the Timepix [14] or the Beetle [15]. HDMI cables connect the hybrid to the core of the SRS: a user-specific adapter card connected to the SRS common Front-End Concentrator (FEC, see Section 2.3). A total of eight hybrids can be connected to one adapter card. A Gigabit Ethernet connection between the FEC and a computer is established either directly or via an Ethernet switch. The components of this local network using standard Ethernet UDP communication are several FECs, each with a unique IP and the computer. User-specific data acquisition and slow control software is used to operate the SRS. Optionally instead of a switch, a Scalable Readout Unit (SRU) is available, in which the data of up to 40 FECs are combined. The scalability of the system is achieved by the fact that several hybrids can be connected to one FEC and several FECs can be connected to a computer.

2.1. The hybrid

The interface between detector and readout electronics is the hybrid. It connects a specific readout ASIC to the detection elements and provides the input needed by the chip as for example power, clock and slow control signals and transmits the data to the adapter card.

2.2. The adapter card

As the hybrid, the design of the adapter card is specific to the front-end ASIC employed. By default, the connection to the hybrids is provided by HDMI cables for most implementations. Depending on the type of front-end technology (analogue, digital, pixel ASIC), the components and logic on the adapter card may vary significantly. The adapter card connects to the FEC via one or two PCI connectors depending on its size and the specific implementation.

2.3. The front-end concentrator card

As core of the back-end, the FEC [16] provides communication with a computer by Gigabit Ethernet. The FEC card front-panel implements 2 × RJ45 for trigger and external clock, 2 × SFP as data links, 2 × LEMO-50 Ω trigger in- and outputs, 1 × differential multi-purpose input and a 9-way connector for power as can be seen in Fig. 5 in Section 4.2. Up to eight FECs can be housed in a 19-inch ATX-powered Eurocard chassis.

The FEC card holds power converters, flash memory, a slot for a DDR3 memory and a Virtex-6 FPGA [17] . The firmware of the FEC is individual for different types of front-ends.

3. The VMM ASIC

For the readout of the NSW detectors, a new front-end ASIC, the VMM is developed by BNL. The design is driven by the detector characteristics and the timing and resolution requirements given by the physics and trigger scheme of the ATLAS experiment. The first version of the ASIC was available 2012 and extensively tested with different detectors [5,18,19]. After the second version VMM2 [20] in 2014 and VMM3 in 2016, first quantities of the final ASIC VMM3a have become available at the beginning of 2018.

The VMM ASIC is designed in 130 nm technology and has 64 input channels, each with a preamplifier, shaper, a peak detector and several ADCs. The digitised data set of 38 bits per hit is multiplexed and can be read out on two lines double data rate with a clock frequency of up to 200 MHz. The chip can be programmed via two digital lines (data and clock).

As in the application in the NSW, positive as well as negative charge will be detected, the analogue part is designed for both polarities. Due to the different charge collection elements such as pads, anode strips and wires, detector capacitances between a few pF and 3 nF can be handled. The input charge acceptance ranges from 0.1 pC to 2 pC with a resolution smaller than 1 fC rms. A time resolution below one nanosecond is foreseen.

The chip is designed with low power consumption and can be programmed for a wide range of applications due to an adjustable gain, peaking time, polarity, threshold and timing precision. It includes a dedicated test pulse circuit per channel and single-channel threshold trimming.

Only the arrival time (time at the peak or time of threshold crossing) and amplitude of the analogue input signal are measured, digitised and multiplexed with the number of the channel hit into a data stream. For triggering, the channel number of the first hit is provided with a minimal delay (address in real time, ART). Additionally for each channel, a direct and fast digital output signal can be generated, which can be the Time over Threshold (ToT), Time to Peak (TtP), Peak to Threshold (PtT), Peak to Peak (PtP) or a 6-bit low-resolution ADC value of the amplitude with a conversion time of 25 ns.

Fig. 2 illustrates the treatment of an analogue signal over threshold in the VMM in case of a configuration to measure the arrival time at the peak position. To measure the amplitude, the Peak Detector Output (PDO) signal rises with the input pulse. When the peak is detected, PDO stays at this level and the amplitude is later digitised by a 10-bit ADC.

For timing, a voltage ramp of the Time Detector Output (TDO) starts to increase linearly from the time of the peak until the next falling edge of a clock. The same clock also increments a 12-bit counter, which serves as coarse timing. For the fine timing between clock cycles, the value of TDO is digitised by an 8-bit ADC.

The VMM has an option to enable the readout of data from channels, for which the threshold has not been reached, but which are adjacent to a channel with a signal over threshold, a so called neighbouring logic. This way, shared charge can still be detected, even though it is not enough to surpass the threshold.

After the conversion time (in the order of 250 ns), the channel is reset and the data set (38 bits per hit) is latched onto a four hit deep buffer in continuous mode. Theoretically, the per channel hit rate reaches up to 4 MHz, which however can be reduced by the return to baseline in the analogue part of the ASIC. By using a token scheme, the data set is pushed out of the VMM on two data lines by another clock (CKDT).

4. SRS + VMM developments

In a similar way as for the other ASICs, the VMM chip has been implemented in the SRS. Following the SRS requirements to implement a new chip, FPGA firmware, an adapter card and a hybrid to be connected to the detector have been designed. These components are explained in this section.

4.1. RD51 VMM hybrid

To implement the VMM in the SRS, the front-end ASIC is placed on a hybrid, which is the first part of the electronics chain and directly connected to the detector. Each input channel is spark-protected via a TVS diode IC [22] and AC-coupled to an input of the VMM, see Fig. 3.

For interchangeability with the established APV25 hybrid, two VMM ASICs are placed on one VMM hybrid as can be seen in Fig. 4, such that 128 channels can be read out as with the APV25. The PCB also holds