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C2D8: An eight channel CCD readout electronics dedicated to low energy neutron detection

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ABSTRACT

Position-sensitive detectors for cold and ultra-cold neutrons (UCN) are in use in fundamental research. In particular, measuring the properties of the quantum states of bouncing neutrons requires micro-metric spatial resolution. To this end, a Charge Coupled Device (CCD) coated with a thin conversion layer that allows a real time detection of neutron hits is under development at LPSC. In this paper, we present the design and performance of a dedicated electronic board designed to read-out eight CCDs simultaneously and operating under vacuum.

1. Introduction

Neutrons interact with matter mostly through strong nuclear interaction. When the neutron wavelength becomes commensurate with the inter-atomic spacing, only coherent scattering occurs. As a consequence, neutrons slowed down to kinetic energies below 100 neV are totally reflected at any angle of incidence by most solid surfaces. These *ultra-cold neutrons* constitute a sensitive tool to study fundamental interactions and symmetries [1]. In particular, ultra-cold neutrons are used to study gravity in a quantum context [2–5]. A neutron bouncing on top of an horizontal mirror realizes a simple one dimensional quantum well problem and the vertical motion of the neutron bouncer has discrete energy states. The wave functions associated to the stationary quantum states have a spatial extension governed by the parameter $z_0 = (\hbar^2/2m_n^2 g)^{1/3} \approx 6\,\mu m$. Therefore, observing the spatial structure of the quantum states requires position-sensitive neutron detectors with a micro-metric spatial resolution.

Semiconductor-based detectors, coated with adequate neutron converters, have been demonstrated to be well suited for this kind of measurements [6–9]. The UCNBox (Ultra Cold Neutrons BOron piXels) detector has been recently developed as position sensitive sensor optimized to measure the wave-functions of the bouncing neutron in the GRANIT experiment [10]. The GRANIT facility uses a 30 cm wide glass mirror as the surface where neutrons bounce. The setup is inside a vacuum chamber at 10^{-5} mbar. The detector, composed of 8 Charge Coupled Devices (CCD), is designed to cover a sensitive area of 300 mm × 0.8 mm. Each CCD is an Hamamatsu S11071-1106N sensor (pixel size 14 μm × 14 μm and number of effective pixels 2048 × 64) coated with ^{10}B, thanks to plasma assisted physical vapor deposition [11].

Neutron capture on boron produces in most cases both a 1.5 MeV α particle and a 0.8 MeV ^{7}Li nucleus. The CCD sensor is used as a pixelated silicon detector. The charge produced by the energy deposition migrates in the neighboring pixels allowing a precise reconstruction of the position using weighted average. To limit this migration of charges each CCD sensor must be read at approximately a 1 Hz rate, with a dead-time as low as possible. In this project we aimed at dead-times below 1%. The UCN rate in the final experiment should not exceed 1 Hz per sensor. Nevertheless, for calibration purposes, rates as high as 50 Hz per sensor are desirable. Also, given the fact that no mechanical shutter system can be used to avoid neutron detection, the shortest possible readout time must be achieved for each CCD to avoid neutron detection during the CCD charge transfer, as it would corrupt the data. Consequently, the CCD must be read-out at the maximum speed specified by the manufacturer (10 MHz), they can however be read one after another.

Typically, both detection-rate and number of hit pixels are low as all charges from one charged particle are collected within a 11 × 11 pixels matrix. For a maximum rate of 50 Hz per sensor, only 5% of the sensor contains useful data. In normal conditions, this drops to 0.1%. This calls for the implementation of a data reduction system, that removes any pixel data below a discrimination threshold.

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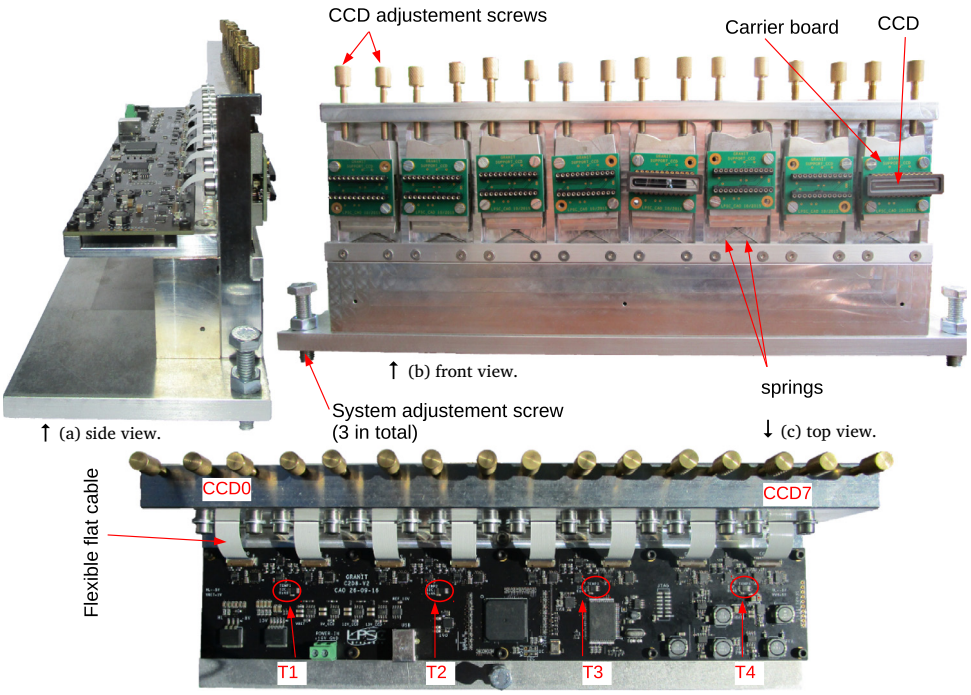

Fig. 1. Picture of the readout electronics mounted on its mechanical support. The electronic system is composed of two parts: the front-end composed of 8 carrier boards, each holding a CCD, and the back-end with the control and readout circuits. The boards are mounted on a mechanical support system equipped with adjustment screws to allow the adjustment of each CCD carrier board position. The four thermal sensors implemented on the board are indicated (T1 to T4).

It must be noted, that an adjustable exposure time must be implemented to permit the use of bright light sources such as LED used to test and adjust CCD alignment.

Additionally, the readout system must be located very close to the sensor system in order to minimize signal integrity issues, but also to minimize the number of vacuum feed-through for the CCD signals (control and readout). This requirement, implies that the readout must be located inside the detector cell and thus withstand vacuum conditions. Consequently, special care must be taken on power usage and heat dissipation to ensure proper operation. This paper is organized as follows: Section 2 presents the hardware design, Section 3 describes the firmware architecture. Eventually, a short summary is given in Section 5.

2. Hardware description

To meet the requirements listed in Section 1, we have opted for a solution based on two distinct modules: a front-end part composed of 8 boards, each holding a CCD; a back-end part for the control and readout circuits. As shown in Fig. 1, the front-end (FEB) and back-end boards are mounted on a common mechanical support. This support is designed such as to be able to finely adjust the position of each CCD board, thanks to dedicated screws. We have checked that this system allows for a relative alignment of the 8 CCDs within 10 µm, sufficient for our needs.

Additionally, the electronics and the support system were designed to optimize the thermal coupling. Indeed, the support system is used to conduct a significant part of the heat flow to the vacuum vessel, while the remaining part of the heat is radiated in the chamber.

A block diagram of the electronics is shown in Fig. 2. Each FEB is connected to the back-end board with a Flexible Flat Cable (FFC). The back-end board is in charge of generating the adequate CCD control signals (horizontal/ vertical shifts and reset gate); performing the CCD signal digitization; aggregating the data and finally making them available for readout via a Universal Serial Bus (USB) interface.

Each CCD signal digitization is carried-out by a dedicated CCD signal processor (Analog devices ADDI7100 [12]). This CCD processor can operate at 45 MHz, which is significantly faster than the maximum readout speed of the Hamamatsu S11071-1106 CCD (10 MHz), and has a digitization resolution of 12 bit with noise performance better than the CCD performance.

Indeed, the CCD processor is specified for having a system noise equivalent to 24.4 e^- (0.8 LSB rms with CDS gain set at +6 dB for a typical CCD sensitivity of 8 µV/e- which corresponds to 30.5e^-/ADU) while the typical CCD noise is composed of the readout noise (23 e^- rms) and of the dark current integration (typically 50 e^-/pixel/s at 25 °C) resulting in a total of 73 e^- for 1 s of integration. The total expected system noise is thus dominated by the CCD and is about 77 e^-, which is compatible with the measurements that showed a system noise of 91.5 ± 15 e^-.

The control signals required to read-out the CCD are generated by a Field Programmable Gate Array (FPGA). These signals, composed of Horizontal/Vertical (H/V) shifting signals and Reset Gate signals (RG), are amplified by dedicated drivers to accommodate the CCD load. The FPGA is also used to produce the signals necessary to operate the CCD signal processor, i.e. clamping and pre-blank signals, the correlated double sampler (CDS) signals and the serial control links.

The rationales for selecting the FPGA used in this design (Xilinx XC7A35-FGG484) were (i) its low power consumption; (ii) the possibility to precisely adjust the timing of the generated signals; (iii) the large amount of memory available. Indeed, the power had to be minimized by design as much as possible to permit the electronics operation under vacuum while avoiding a too fancy mechanical setup for thermalization (for instance: usage of the standby modes of the CCD processors during the exposure time). Additionally, this FPGA features high performance serializers in each of its input/output block. Thanks to these blocks, one can adjust output signals with a time resolution of about 2 ns by using a high speed 480 MHz clock (see Section 3). This makes it possible to conveniently set the CDS sampling times. The sizing of the memory was based on the criteria that its capacity should be at least half of the memory required to buffer the data generated by one CCD readout, i.e. $2048 \times 64/2 = 65{,}536$ 16-bits words, corresponding to more than 1 Mbit of storage. This time equivalent buffering must be considered