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# Development of a time-to-digital converter ASIC for the upgrade of the ATLAS Monitored Drift Tube detector

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ABSTRACT

The upgrade of the ATLAS muon spectrometer for the high-luminosity LHC requires new trigger and readout electronics for various elements of the detector. We present the design of a time-to-digital converter (TDC) ASIC prototype for the ATLAS Monitored Drift Tube (MDT) detector. The chip was fabricated in a GlobalFoundries 130 nm CMOS technology. Studies indicate that its timing and power dissipation characteristics meet the design specifications, with a timing bin variation of ±40 ps for all 48 TDC slices and a power dissipation of about 6.5 mW per slice.



## 1. Introduction

### 1.1. Current MDT and electronics

The ATLAS muon spectrometer [1] is composed of precision tracking and trigger chambers. Precision measurements of the muon track coordinates are provided by three stations of Monitored Drift Tube (MDT) chambers up to $|\eta| = 2.5$.[2] Cathode strip chambers (CSC) with higher granularity are used in the innermost station covering $2.0 < |\eta| < 2.7$. Resistive plate chambers (RPC) located in the barrel region ($|\eta| < 1.05$) and thin gap chambers (TGC) in the endcap region ($1.05 < |\eta| < 2.4$) are used to provide trigger information.

The MDT system is the main component of the ATLAS precision muon tracking system and is designed to provide a stand-alone muon transverse momentum measurement with a resolution of 10% for 1 TeV muons. There are 1150 MDT chambers made from 354 000 aluminum tubes covering a total area of 5500 $m^2$. The chambers have been operated successfully since 2009 and have made important contributions to the discovery of the Higgs boson, precision Standard Model measurements and exotic searches at ATLAS.

Each tube has an inside diameter of 29.97 mm and is filled with a mixture of $Ar/CO_2$ (93/7) at 3 bar. A 50 μm gold-plated tungsten wire is positioned at the center of each tube. A high voltage of 3.08 kV is imposed across the tube wall and the central wire. Ionization created by the passage of a muon track can take up to 750 ns to reach the anode wire.

The present MDT readout electronics [2] is designed to preserve the inherent measurement accuracy of the tubes (80 μm) and to cope with the high hit rates expected at the full LHC luminosity. Raw signals from 24 tubes are routed via signal hedgehog boards and processed by three custom-designed monolithic Amplifier–Shaper–Discriminator (ASD) chips [3]. The differential output signals from the ASDs are then routed to a Time-to-Digital Converter (TDC) chip [4], where the arrival times of leading and trailing edges are digitized and stored in a buffer waiting for the ATLAS first-level trigger accept signal. Each frontend mezzanine card contains three 8-channel ASDs and one 24-channel TDC. Up to 18 mezzanine cards are controlled and readout by an FPGA on the Chamber Service Module (CSM). The CSM communicates with the off-chamber electronics via two optical fibers, one coming from the Timing, Trigger and Control distribution box [5] and the other going to the MDT Readout Driver (MROD) [6].

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[2] ATLAS uses a right-handed coordinate system with its origin at the nominal interaction point in the center of the detector and the $z$-axis along the beam pipe. The $x$-axis points from the IP to the center of the LHC ring, and the $y$-axis points upward. The pseudorapidity is defined in terms of the polar angle $\theta$ as $\eta = -\ln\tan(\theta/2)$.

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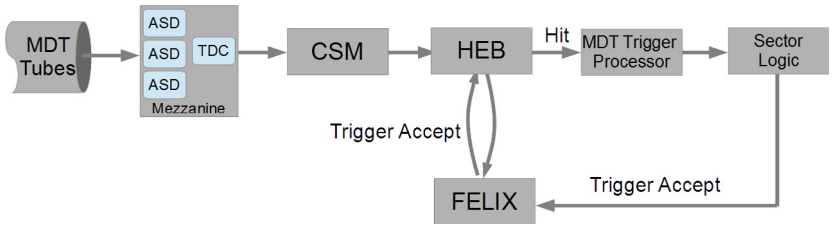


**Fig. 1.** Schematic diagram of the MDT trigger and readout system at the HL-LHC.

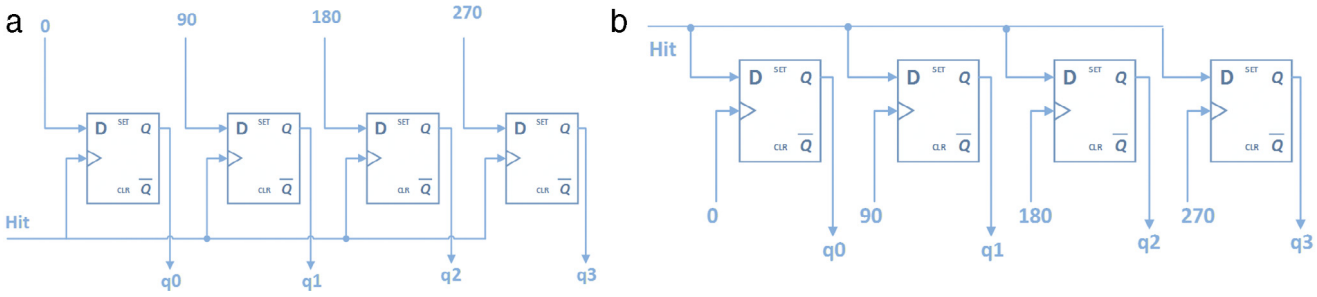


**Fig. 2.** Implementation of the fine time measurement of the TDC. (a) Hit samples clocks; (b) clocks sample Hit.

### *1.2. MDT frontend electronics for high-luminosity LHC (HL-LHC)*

The LHC collider has a few upgrades scheduled in the years 2019–2024 with the instantaneous luminosity increased to $5 - 7.5 \times 10^{34}$ $cm^{-2}$ $s^{-1}$. The machine is expected to collect about 3000 $fb^{-1}$ of data by 2035. ATLAS detector will have corresponding upgrades to its trigger and readout systems to handle the large data rates and demanding environment imposed by these LHC upgrades.

To handle large number of background hits and low momentum muon tracks expected at the trigger level, ATLAS plans to include MDT chamber data in the first trigger level to provide additional rejection of fake muons and to reject low momentum muons by sharpening the trigger turn-on curve. The design of the MDT on-chamber electronics system for the HL-LHC is based on sending all muon hits off chamber to new trigger and readout circuitry in the ATLAS counter room. In this trigger-less scheme, all raw tube signals are amplified, shaped, discriminated, and digitized on the chamber and sent via the CSM to a Hit Extraction Board (HEB). Due to the long drift time of the MDT signal, the timing information from the fast trigger chambers (RPCs in the barrel and TGCs in the endcap) are used as the muon reference time. The fast trigger chamber reference time is used to select possible MDT candidate hits and to convert the observed times to a reduced resolution radial position in the tubes. The radial position information for all matched hits are sent to the MDT trigger processor, where the segment-finding and track-fitting algorithms are performed. Meanwhile, the full-resolution time information for all matched hits are stored for transmission to the FELIX [7] once the first-level trigger accept signal is received. Simulations have demonstrated that this design meets the desired performance with higher data bandwidth.

Fig. 1 shows the overall diagram for the MDT trigger and readout system at the HL-LHC. The TDC is a crucial component in the new trigger architecture. It is responsible for the time digitization of raw tube signals, which is the basis for all following trigger processing. Although the existing TDC [4] has a trigger-less mode, it cannot meet the requirement at the HL-LHC due to the increased data rate. Moreover, the new TDC must also correct the issues found for the present TDC introduced by very narrow pulses at the inputs [8]. This paper focuses on the design of a new TDC targeted for the ATLAS MDT chambers at the HL-LHC.

## 2. Design of a trigger-less TDC for the ATLAS MDT upgrade

In the MDT trigger and readout system, raw signals from a group of 24 tubes are processed by three custom-designed ASDs, from which the timing information is extracted in the form of "Time-Over-Threshold" (TOT) pulses. The leading and trailing edges of the TOT pulses are digitized by a TDC with a bin size of ~780 ps and a dynamic range of one LHC orbit cycle (~102.4 us). This corresponds to a 17-bit time measurement. In addition, the power dissipation of the TDC is also restricted to be less than 350 mW as there is no active cooling system available.

We implement the TDC by breaking the time measurement into coarse-time and fine-time measurements. The dynamic range is covered by the coarse-time measurement while the resolution is achieved from the fine-time measurement. The full range of the fine time measurement is required to cover one single coarse time step, and in total a 17-bit time measurement is assembled. The fine time resolution is derived from interpolation of multiple clock phases, and the fine time measurement is obtained by sampling phase-shifted clocks with the TDC inputs, as shown in Fig. 2(a). In contrast to sampling hits with the phase-shifted clocks (as illustrated in Fig. 2(b)), the proposed architecture is simpler, requires less logic, and consumes less power. This is because the samples from the implementation in Fig. 2(b) are in different clock domains and additional circuits are needed to adapt the samples into the same domain for data processing.

The phase difference between the clocks is ~780 ps and the number of phases is determined by the operating clock frequency of the coarse-time measurement. A higher frequency results in fewer number of phases for the fine-time interpolation whereas more bits in the coarse time measurements will be needed to cover the dynamic range. The choice we made for the TDC using the 130 nm CMOS technology is 320 MHz so that only four phases are necessary, i.e. 0°/90°/180°/270°. Since the phases differ by 90 degrees, in principle two clocks with a phase shift of 90° is adequate if we make use of both rising and falling edges. The bit width for fine-time and coarse-time measurements are thus 2 bits and 15 bits respectively. A 50% duty cycle of the clock is crucial for the timing uniformity. The final time measurement of a hit is a combination of the coarse-time and fine-time measurements.