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Improvement to the signaling interface for CMOS pixel sensors

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ABSTRACT

The development of the readout speed of CMOS pixel sensors (CPS) is motivated by the demanding requirements of future high energy physics (HEP) experiments. As the interface between CPS and the data acquisition (DAQ) system, which inputs clock from the DAQ system and outputs data from CPS, the signaling interface should also be improved in terms of data rates. Meanwhile, the power consumption of the signaling interface should be maintained as low as possible. Consequently, a reduced swing differential signaling (RSDS) driver was adopted instead of a low-voltage differential signaling (LVDS) driver to transmit data from CPS to the DAQ system. In order to increase the capability of data rates, a serial source termination technique was employed. A LVDS/RSDS receiver was employed for transmitting clock from the DAQ system to CPS. A new method of generating hysteresis and a special current comparator were used to achieve a higher speed with lower power consumption. The signaling interface was designed and submitted for fabrication in a 0.18 μm CMOS image sensor (CIS) process. Measurement results indicate that the RSDS driver and the LVDS receiver can operate correctly at a data rate of 2 Gb/s with a power consumption of 19.1 mW.

1. Introduction

High energy physics experiments at particle accelerators set stringent requirements on the performances of vertex detectors in terms of spatial resolution, material budget, readout speed, radiation tolerance and power consumption [1–4].

For some vertex detectors, CMOS pixel sensors (CPS) are particularly promising [5,6]. CPS exploit standard CMOS processes to integrate a full signal processing chain on the same substrate as the sensing element, as shown in Fig. 1. Due to this intrinsic operation principle, CPS feature high granularity and thin sensitive volume. The feasibility of using CPS for charged particle tracking was demonstrated by the development of the EUDET beam telescope [7]. In addition, the vertex detector (called PXL) of the upgraded inner tracking system of the solenoidal tracker at RHIC (Relativistic Heavy Ion Collider) (STAR) experiment is based on CPS [8,9]. The upgrade of the inner tracking system (ITS) of a large ion collider experiment (ALICE) (shown in Fig. 2) entirely based on CPS has been approved [10]. Nevertheless, CPS should still prove their conformity in terms of readout speed for some detectors, such as the micro vertex detector (MVD) of the compressed baryonic matter (CBM) experiment, and the international large detector (ILD). In addition, the radiation tolerance of CPS should also be improved [5,6]. These motivate the development of a new generation of CPS with a new high rate (up to ~Gb/s) [11] transmission circuitry in a low power supply technology.

For clock and data transmission of CPS, low-voltage differential signaling (LVDS), as shown in Fig. 3, is a quite attractive and commonly used technology [12,13]. Owing to its small output swing, current steering and differential signaling, LVDS can achieve data rates up to several Gb/s with low power, low noise generation, and excellent noise immunity [14]. However, the LVDS interface could be substituted with a reduced swing differential signaling (RSDS) [15] interface to better suit the application of CPS. Since the transmission distance for the application of CPS is relatively short, power consumption of the interface of CPS could be reduced by adopting RSDS instead of LVDS. Although the maximum data rate of RSDS is limited compared to LVDS as signal swings are reduced, it could be mitigated by introducing a serial source termination technique, a new method for generating hysteresis, and a special current comparator. In addition, the occupied area of the interface could be reduced because smaller transistors are used for the RSDS interface due to smaller driving current, which indicates a smaller dead zone for the detection of the charged particle tracking.

This work focused on the improvement in the data rate of the signaling interface for CPS up to Gb/s with minimum increase in power consumption and a small occupied area. The paper is organized as follows. The design of the driver and the receiver is presented in Sections 2 and 3 respectively. Section 4 is dedicated

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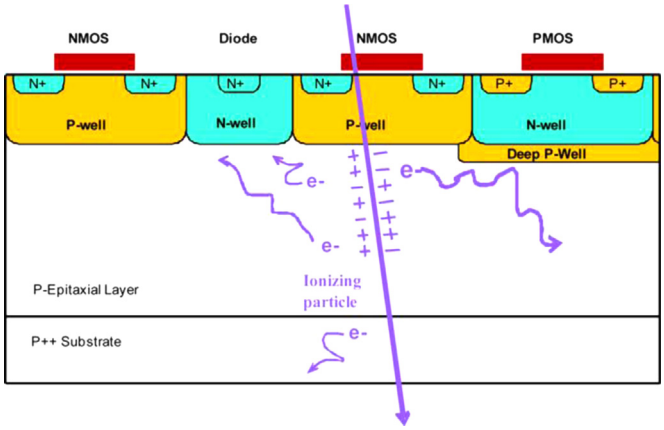

Fig. 1. Operation principle of CPS.

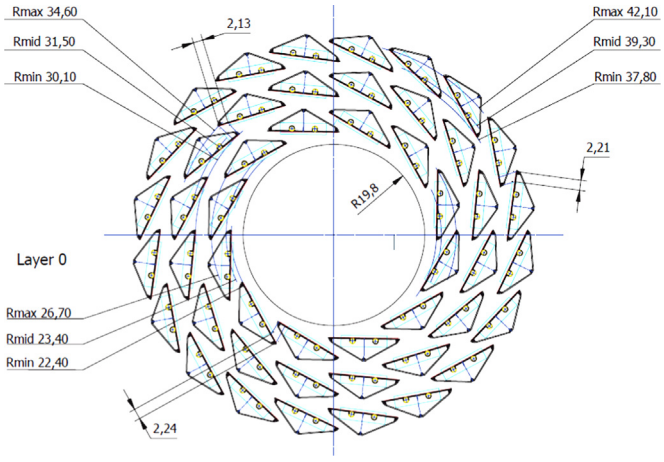

Fig. 2. Schematic view of the cross section of the ALICE ITS Inner Barrel.

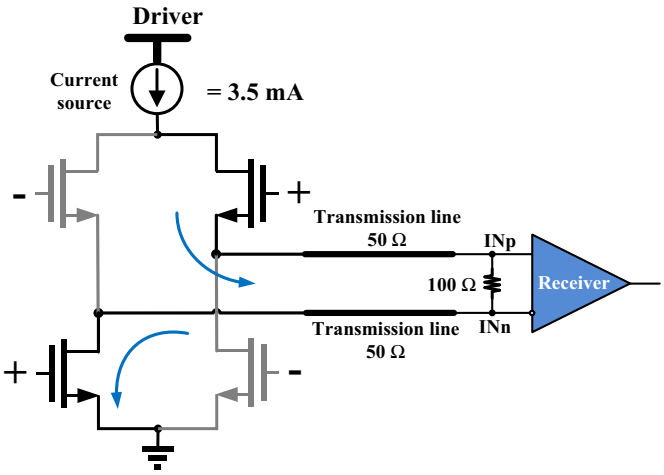

Fig. 3. Typical LVDS driver and receiver.

to the implementation of the layout in a 0.18-μm CMOS image sensor (CIS) process and measurement of the circuitry. Finally, the paper is concluded in Section 5.

2. Driver design

The RSDS driver is used to convert CMOS signals to RSDS signals and then transmit the RSDS signals from CPS to the DAQ

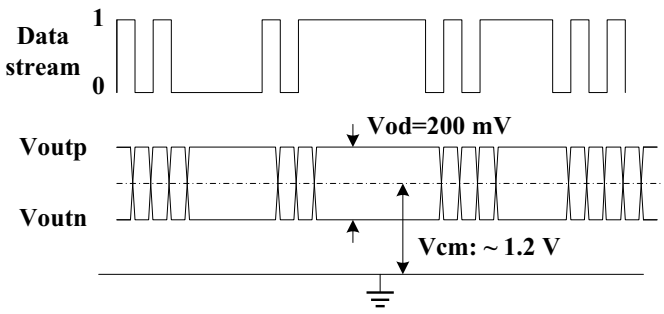

Fig. 4. Output signals of an RSDS driver.

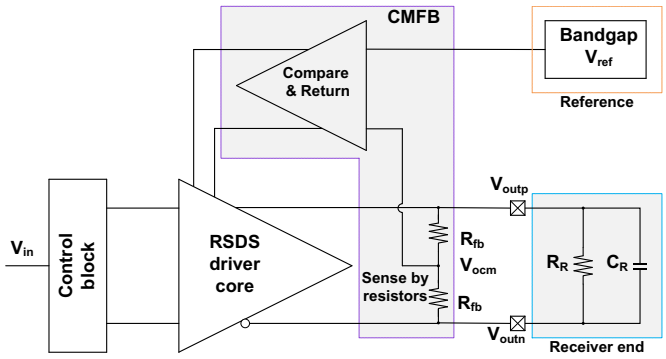

Fig. 5. Typical RSDS driver block diagram.

system outside CPS. Typical RSDS signals are shown in Fig. 4. The function of the RSDS driver is implemented by the architecture shown in Fig. 5. It is composed of a control block, a driver core block, and a common mode feedback (CMFB) block. The control block converts CMOS single-ended input signals to differential signals and generates control signals for the driver. The driver core block delivers an output current, the polarity of which corresponds to the output differential signals of the control bock. A schematic of a typical driver core is shown in Fig. 6(a). This circuit is composed of four MOS switches (M2–M5) arranged in a bridged configuration. If the input is positive, M2 and M5 are turned on while M3 and M4 are turned off, forming a current path from the power supply to ground. Thus, current flows from the positive output node (V_{outp}) to the negative output node (V_{outn}), leading to a positive output voltage. On the contrary, if the input is negative, then the polarity of the output current and voltage is reversed. The CMFB circuit allows for the stabilization of the driver's output common mode voltage at the reference voltage (V_{ref}). This voltage is generated from a bandgap reference to be insensitive to process–voltage–temperature (PVT) variations.

The main difference of typical signals between RSDS and LVDS is summarized in Table 1. Since its output driver current is less than that of LVDS, RSDS consumes a smaller amount of power. However, the maximum data rate of RSDS is also limited compared to LVDS as output signal swings are reduced.

The limitation of the maximum data rate of RSDS could be mitigated by improving the signal integrity of RSDS output signals. The techniques adopted in LVDS drivers, such as the open-drain configuration [16], the double current source [17], and the parallel source termination [18] could be applied in the design of LVDS drivers. However, all of those techniques mentioned above improve the data rate at the cost of dramatic increase in power consumption, which weakens the advantage of RSDS.

The serial source termination technique [19,20] is adopted in the design of the RSDS driver to increase the maximum data rate. By providing impedance matching between the source and the