Nuclear Instruments and Methods in Physics Research A ∎ (∎∎∎∎) ∎∎∎–∎∎∎

Contents lists available at ScienceDirect

Nuclear Instruments and Methods in Physics Research A

journal homepage: www.elsevier.com/locate/nima

First results of a Double-SOI pixel chip for X-ray imaging

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ARTICLE INFO

Article history:
Received 17 November 2015
Received in revised form
29 February 2016
Accepted 8 April 2016

Keywords:
SOI pixel detector
Crosstalk
Counting-type

ABSTRACT

Aiming at low energy X-ray imaging, a prototype chip based on Double-SOI process was designed and tested. The sensor and pixel circuit were characterized. The long lasting crosstalk issue in SOI technology was understood. The operation of pixel was verified with a pulsed infrared laser beam. The depletion of sensor revealed by signal amplitudes is consistent with the one revealed by *I–V* curve. An s-curve fitting resulted in a sigma of 153 e^- among which equivalent noise charge (ENC) contributed 113 e^-. It's the first time that the crosstalk issue in SOI technology was solved and a counting type SOI pixel demonstrated the detection of low energy radiation quantitatively.

1. Introduction

The Silicon on Insulator (SOI) process is an established technique for transistor isolation. Pixelated radiation detectors based on SOI process was first proposed for tracking of charged particles [1,2]. It's also gaining popularity in X-ray imaging since a high resistive handle wafer allows depletion layer thickness up to several hundred microns [3–5]. We are pursuing a counting type pixel array with extreme fine pitch, moderate number of bits in counter and excellent signal/noise ratio. The ultimate goal is 30 μm pitch, 14-bit counter per pixel and signal/noise ratio (S/N) sufficient to detect low energy photons down to 2 keV, which is required by the study of materials in synchrotron experiments.

To achieve the specified S/N, we need to understand the crosstalk, an intrinsic issue in SOI technology [6]. The strong capacitive coupling between the sensor and pixel circuit leads to large crosstalk. A voltage transition in pixel circuit would induce thousands of electrons on the charge collection electrodes in the sensor. Other groups had studied different shielding methods but achieved limited success [7,8].

We use Double-SOI wafers and related processes developed by the KEK group and industrial partners [9]. To evaluate the shielding effectiveness of Double-SOI, we designed a prototype chip CPIXTEG3b which contains diode array and complete electronics. Basic characterization of the chip will be reported with an emphasis on the shielding of crosstalk. A laser test system was used as a source of radiation, which features pico-second pulse duration, repeating rate up to 1 MHz, and adjustable single pulse power ranging from 0.01 pJ to 60 pJ [10].

2. Double-SOI process

Double-SOI serves two purposes, to compensate the trapped charge in the buried oxide (BOX) layer and to shield the crosstalk between the sensor and the circuit. The trapped charge is not a concern in our case of low energy X-ray imaging, provided the chip is illuminated from the handle wafer side.

Double-SOI wafer has an additional device layer, the SOI2 layer, as a dedicated shielding layer. As shown in Fig. 1, the diode array is formed by buried N-well (BNW) at the top side of handle wafer (P-type with a nominal resistivity > 1 kOhm cm). Each diode is connected to the preamplifier via the BNW contact. The handle wafer is originally 725 μm thick and usually thinned to 300 μm before a common anode on its backside is formed by P+implantation and aluminum sputtering. The device layer SOI1 accommodates transistors while the shielding layer SOI2 is grounded via the SOI2 contact. The capacitive path between transistors and charge collection electrodes is cut off by SOI2, which eliminates the pickup of disturbance from active transistors. In addition, the "blanket" of SOI2 provides uniform potential distribution underneath all transistors, which is important for suppressing back-gate effect and maintaining the threshold of transistors.

However, SOI2 has a high sheet resistance about 30 kOhm/square due to its thinness. Increasing the density of SOI2 contacts is required to compensate the resistance but it occupies considerable area in the crowded pixel. The excessive

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http://dx.doi.org/10.1016/j.nima.2016.04.022
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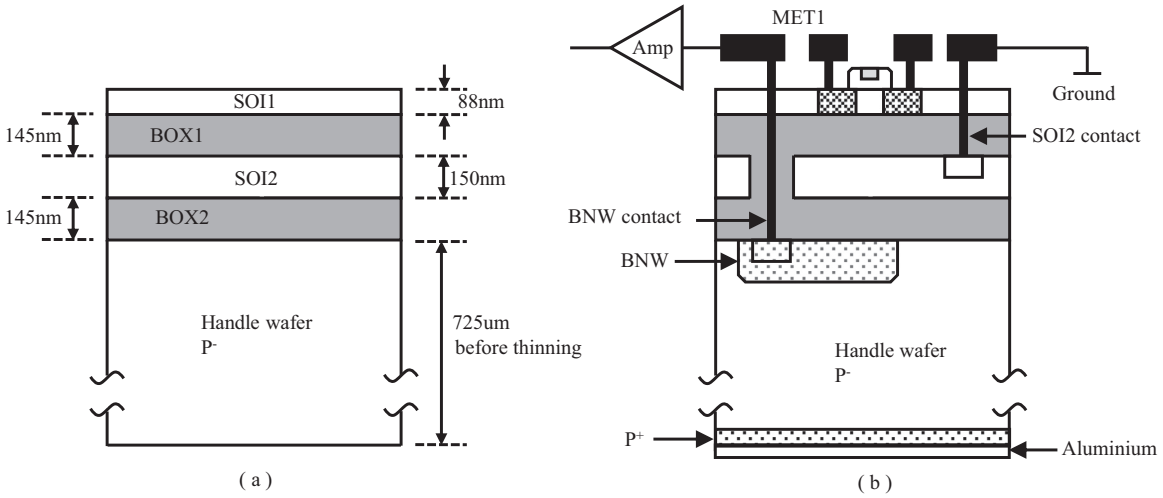

Fig. 1. Schematic view of a simplified cross-section of Double-SOI. The Left and right panels represent Double-SOI wafer before and after processing respectively. The stack-up consists of 2 device layers SOI1 and SOI2, 2 dioxide layers BOX1 and BOX2, and the high resistive handle wafer with their thickness indicated in the graph (not to the scale).

capacitance to BNW is another pain inflicted by SOI2 which adds to the equivalent input capacitance for preamplifier and therefore degrades S/N.

3. Description of the prototype chip

The prototype chip CPIXTEG3b measures $6 \times 6\ \mathrm{mm}^2$, which includes a sensitive area of $3.2 \times 3.2\ \mathrm{mm}^2$. The pixel array consists of 64×64 identical cells except for a few of those were modified for basic characterization. In-pixel signal processing and peripheral bias and controls were designed with a 0.2 μm CMOS process.

3.1. On-chip electronics

The upper panel of Fig. 2 shows the circuit blocks in one pixel. The charge sensitive preamplifier integrates the negative current of N-in-P sensor where the voltage pulse amplitude is proportional to the signal charge. The signal gets amplified further by the shaper and discriminated by a voltage comparator. Only the signals larger than the preset threshold are registered by the counter. The 6-bit counter is read out through a sequential chain at the interval of exposure period.

All the current sources required by various amplifiers in one pixel are copied from the reference current in the peripheral by current mirrors. To measure the accuracy of current sources and the fidelity of analog waveforms, 6 pixel cells were connected to dedicated I/O pads for test as shown in the lower panel of Fig. 2. The 3 cells for current measurement have no buffering, which enables accuracy better than 1 nA. The other 3 for waveform inspection have analog buffers connected to the internal nodes such that the capacitive load of oscilloscope probes would not degrade the waveforms.

3.2. Pixel layout

The pixel layout is shown in Fig. 3. The size of BNW was designed small partly for reducing the capacitance between BNW and SOI2 and partly for avoiding the overlap with counter, the most vigorous source of crosstalk. Meanwhile, the layout of counter must be made as small as possible. Because the area underneath the counter is not covered by the BNW, which degrades charge collection efficiency and increase charge sharing. Therefore, the counter was truncated to 6 bits in this chip and the pixel layout was constrained within $50 \times 50\ \mu\mathrm{m}^2$.

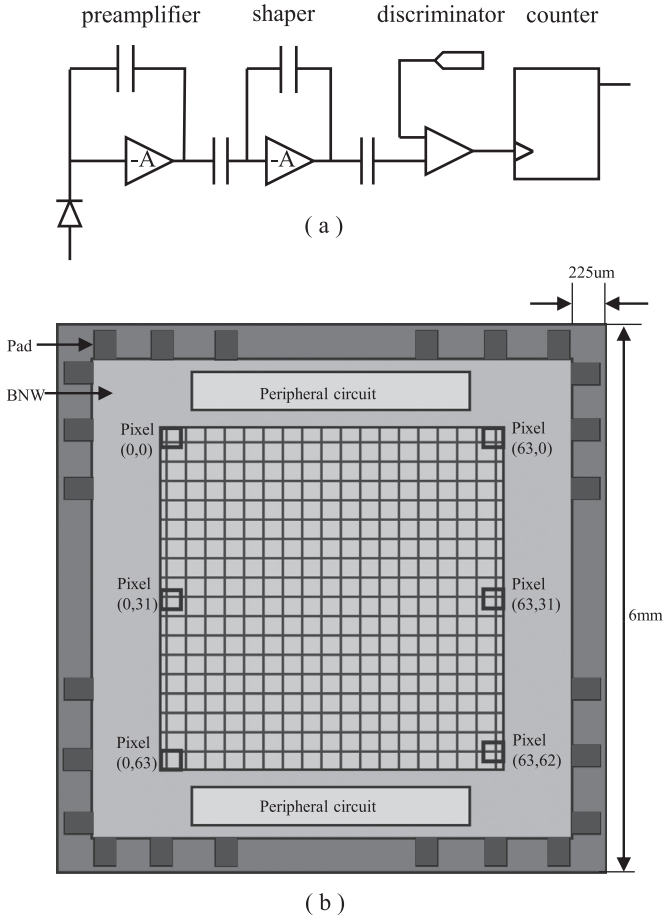

Fig. 2. Circuit blocks in one pixel and sketched floorplan of CPIXTEG3b (not to the scale). The signal current of the sensor is processed by a conventional configuration of preamplifier, shaper and discriminator, and the number of signal pulses is registered by a counter (upper panel). 3 pixel cells in the column 0 are used for waveform inspection and 3 pixel cells in the column 63 are used for measuring the current sources (lower panel).

Two rows of SOI2 contacts were placed to conduct the induced current in SOI2 to the shielding ground and enhance the segregation between BNW and the counter. The shielding ground shared by all pixels is separated from the circuit ground and