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Development of an X-ray imaging system with SOI pixel detectors

Ryutaro Nishimura [a,*], Yasuo Arai [b], Toshinobu Miyoshi [b], Keiichi Hirano [c], Shunji Kishimoto [c], Ryo Hashimoto [c]

[a] School of High Energy Accelerator Science, SOKENDAI (The Graduate University for Advanced Studies), Oho 1-1, Tsukuba, Ibaraki 305-0801, Japan
[b] Institute of Particle and Nuclear Studies, High Energy Accelerator Research Organization (KEK-IPNS), Oho 1-1, Tsukuba, Ibaraki 305-0801, Japan
[c] Institute of Materials Structure Science, High Energy Accelerator Research Organization (KEK-IMSS), Oho 1-1, Tsukuba, Ibaraki 305-0801, Japan

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ABSTRACT

An X-ray imaging system employing pixel sensors in silicon-on-insulator technology is currently under development. The system consists of an SOI pixel detector (INTPIX4) and a DAQ system based on a multi-purpose readout board (SEABAS2). To correct a bottleneck in the total throughput of the DAQ of the first prototype, parallel processing of the data taking and storing processes and a FIFO buffer were implemented for the new DAQ release. Due to these upgrades, the DAQ throughput was improved from 6 Hz (41 Mbps) to 90 Hz (613 Mbps). The first X-ray imaging system with the new DAQ software release was tested using 33.3 keV and 9.5 keV mono X-rays for three-dimensional computerized tomography. The results of these tests are presented.

1. Introduction

X-ray imaging can non-destructively show the internal structure of an object. Therefore, it is used for medical tests, structure analyses of samples, and some industrial applications. In particular, X-ray imaging with synchrotron radiation is used for microstructure imaging because of the characteristics of the light source, which is highly collimated, highly polarized, and energy-tunable. For these measurements, the user needs a sensor with high resolution.

The SOI pixel detector [1] is a Si semiconductor detector with small pixel size (size of the smallest pixel we have developed is $8 \times 8\ \mu m^2$ (FPIX [2])) and can directly transform X-ray energy. Because of these characteristics, the SOI pixel detector is suited for X-ray imaging that requires high spatial resolution (~30 μm). We are developing an X-ray imaging system that uses this SOI pixel detector.

For practical X-ray imaging, the throughput of the DAQ system has been a significant problem. We attempted to solve this problem by refining the DAQ software. We attempted to take X-ray imaging data and X-ray CT data by using this imaging system, and we confirmed our sensor's performance.

1.1. Photon factory

The Photon Factory [3] is an accelerator-based light source facility that is a part of the High Energy Accelerator Research Organization (KEK), Japan. The Photon Factory operates two storage rings: the 2.5 GeV PF Ring and the 6.5 GeV PF Advanced Ring (PF-AR). These two rings supply brilliant X-rays and VUV light. In this study, we attempt to apply the SOI pixel detector as the X-ray imaging sensor, which can be used for brilliant light sources such as the PF.

1.2. SOI detector

SOI pixel detectors (Fig. 1) are being developed by a SOIPIX collaboration led by KEK. They are based on a 0.2 μm CMOS fully depleted (FD-) SOI process of Lapis Semiconductor Co., Ltd [1]. The SOI detector consists of a thick (50–500 μm in Floating Zone type wafer) and high-resistivity (more than 2 kΩ-cm) in Floating Zone type wafer) Si substrate for the sensing part, and a thin Si layer for CMOS circuits [1]. Because an SOI detector has no bump bonds, the application has low capacitance, low noise, high gain, low material budget, and can run fast with low power. The comparison of an SOI pixel detector and Hybrid Pixel detector is shown in Table 1.

For the X-ray imaging system, integration-type SOI pixel detectors named INTPIX4 [4] are used. The pixel size is $17 \times 17\ \mu m^2$, the number of pixels is 832×512, and the sensitive area is $14.1 \times 8.7\ mm^2$. This detector consists of 13 blocks (64×512 pixels/

* Corresponding author.
E-mail address: ryunishi@post.kek.jp (R. Nishimura).

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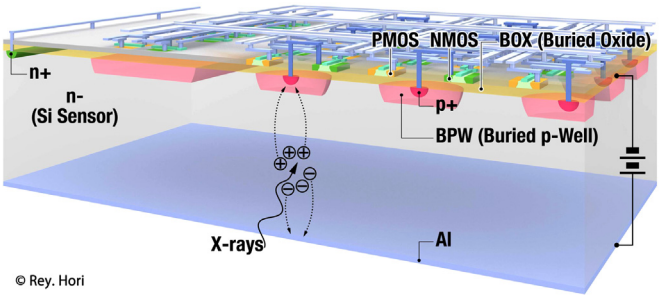

Fig. 1. Structure of the SOI detector.

Table 1
Comparison of SOI pixel detector and Hybrid Pixel detector.

	SOI device	Hybrid device
Pixel size	>8 μm	>50 μm
Material budget	Minimized	Large
Parasitic capacitances	~10 fF	~100 fF

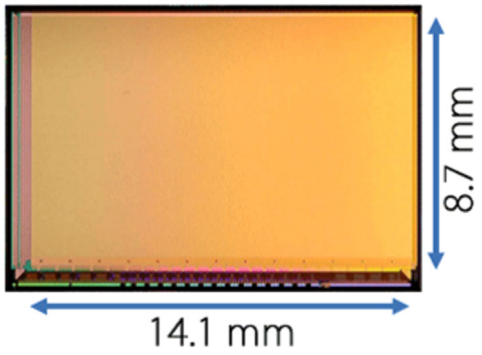

Fig. 2. Photograph of INTPIX4.

block), and each block has independent channels of analog output for parallel readout. A photograph of INTPIX4 is shown in Fig. 2.

1.3. SEABAS DAQ system

INTPIX4 is read out through a board called SEABAS 2 (Soi EvAluation BoArd with Sitcp 2 [5]). SEABAS 2 is the second generation of the SEABAS board.

The signal output by INTPIX4 is an analog signal converted from collected charge. This signal is converted to the count of the A/D conversion Unit (ADU) by the SEABAS2 onboard ADC. After conversion, data are passed to the DAQ PC. The PC and SEABAS2 are connected by Gigabit Ethernet and communicate with TCP/UDP protocol. The transferred data are processed by software that runs on a PC. The schematic diagram of the SEABAS DAQ is shown in Fig. 3.

Fig. 4 shows a photograph of SEABAS 2. This board has 2 FPGAs: one is a SiTCP network processor and the other is a user customizable circuit. This board has a 12-bit 16-channel A/D Converter

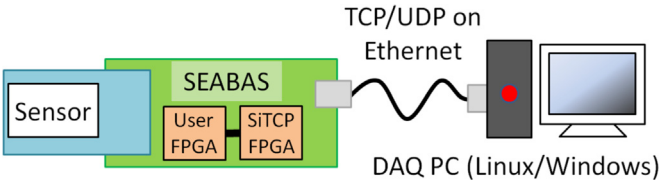

Fig. 3. Schema of SEABAS DAQ system.

(ADC) to convert the detector's analog output. When SEABAS2 transfers INTPIX4's output after ADC conversion, the total data size is 6,815,744 bit (ADC 12 bit+padding 4 bit=16 bit per pixel) per frame.

The SOI Pixel sensor outputs a large quantity of data at a time. For example, it outputs 6,815,744 bit/frame in the case of INTPIX4. Therefore, fast data transfer is important for measurements which need a full pixel scan in a short period.

2. Methods

2.1. Bottleneck in the existing DAQ system

In the INTPIX4/SEABAS2 DAQ system, analog signals read out from INTPIX4 are converted to digital signals in the ADC integrated in SEABAS2. The digital signals are transferred to the DAQ PC via the Ethernet connection. Fig. 5 shows the data flow.

To increase the total throughput, the following three points are important.

1. Convert A/D in a short time. (INTPIX4Sensor - User FPGA).
2. Transport data in a short time. (SEABAS2 - DAQ PC).
3. Ensure that the process of data receiving and the process of data storage do not interfere with each other during data taking. (DAQ PC and inside of DAQ software).

The maximum speed is limited by point 1 because this factor is linked to the hardware (ADC and INTPIX4) specification. The limitation regarding point 1 is shown in Table 2. In this case, INTPIX4's performance is the most significant limiting factor. Thus, the required minimum speed of points 2 and 3 is also set to 80 Hz. The total signal length of pixel data is 16 bit/pixel, the width of the digital signal after A/D conversion of the analog signal is 12bit, and a 4bit readout channel ID is added to the top of the data stream. Therefore, the total required throughput of 80 Hz readout is 545 Mbps.

Here, we predict the transfer speed of the SEABAS DAQ system using the Gigabit Ethernet for transfer. When all measurement data are transferred over ethernet by TCP protocol, the transfer speed that can be used for sensor data is about 95% of the Gigabit Ethernet's maximum speed (1 Gbps). The other 5% is to be used for the structural data of the packet. Furthermore, the prospective transfer speed is approximately 570 Mbps (83.6 Hz)–665 Mbps (97.5 Hz) when the DAQ system can use 60–70% of the theoretical speed. On the other hand, the existing system's transfer speed is 41 Mbps. This means the existing system has some time loss. Most of the time loss is caused by the structure of the DAQ software, in which the processes of data taking and data storage are sequential. Thus, separating the data taking process from other processes will solve this problem.

2.2. Implementation of multi-thread (MT) processing

Multi-thread processing is the refined software approach. The schematic diagram of this approach is shown in Fig. 6.

In the existing system, software works on single-thread processing. In this case, the data taking and data storage processes are sequential. Therefore, the next data taking process has to follow the previous data storage process. Consequently, the net DAQ efficiency is reduced.

This software structure was refined using multi-thread processing. To implement multi-thread processing, WIN32API [6] (Windows) or Posix Thread [7] (Linux) was used. The refined software's structure consists of 2 threads: one is the data taking thread, and the other is the data storage thread. These threads

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