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Reduction of cross-talks between circuit and sensor layer in the Kyoto's X-ray astronomy SOI pixel sensors with Double-SOI wafer

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ABSTRACT

We have been developing silicon-on-insulator pixel sensors, "XRPIXs," for future X-ray astronomy satellites. XRPIXs are equipped with a function of "event-driven readout," with which we can read out only hit pixels by trigger signals and hence realize good time resolution reaching ~10 μs. The current version of XRPIX suffers from a problem that the spectral performance degrades in the event-driven readout mode compared to the frame-readout mode, in which all the pixels are read out serially. Previous studies have clarified that one of the causes is capacitive coupling between the sense node and the trigger signal line in the circuit layer. In order to solve the problem, we adopt the Double SOI structure having a middle silicon layer between the circuit and the sensor layers. We expect the middle silicon layer to work as an electrostatic shield and reduces the capacitive coupling. In this paper, we report the spectroscopic performance of XRPIX with the middle silicon layer. We successfully reduce the capacitive coupling and the readout noise.

1. Introduction

Charge-Coupled Devices (CCDs) are standard imaging spectrometers for X-ray astronomy satellites [1–3]. They offer Fano-limited spectroscopy with their low readout noise and fine imaging with their small pixel sizes of 20 – 30 μm. However, CCDs have a poor time resolution of ~1–10 s. The poor time resolution not only prevents us from observing short-timescale phenomena in the Universe but also limits the background rejection capability. Non-X-ray backgrounds (NXB) are mainly generated by bombardment of in-orbit cosmic-ray particles and limit the detector sensitivity particularly in the hard X-ray band above 10 keV. One of the effective ways of rejecting NXB is to employ anti-coincidence shields surrounding main sensors. The time resolution of CCDs is not good enough to use this technique. Thus, we have been developing silicon-on-insulator pixel sensors (SOIPIXs), "XRPIX," for future X-ray astronomy satellites.

XRPIX contains a comparator circuit in each pixel, the hit row and column address being sent to the trigger logic. The trigger logic examines the hit pixels and generates a trigger if the hit pattern is consistent with the one of X-rays. Thus, the on-pixel comparator circuits are key elements enabling the function of "event-driven readout" and realize good time resolution better than ~10 μs. Therefore, we can reduce NXB with XRPIX by introducing the anti-coincidence method.

SOIPIXs consist of the following three layers: a complementary metal-oxide-semiconductor (CMOS) circuit layer made with low-resistivity silicon, a high-resistivity depleted silicon layer for X-ray detection, and a buried oxide (BOX) layer for insulation between the two layers. Each pixel has a p^+ sense node implanted in the sensor layer and a contact via through the BOX layer which

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connects the sense node with the CMOS circuit. A buried p-well (BPW) is implanted around the sense node for efficient signal charge collection and to suppress the back-gate effect [4].

Takeda et al. [5] reported that spectral performance degrades in the event-driven readout mode compared to the frame-readout mode, in which all the pixels are read out serially like CCDs. One observation is that an offset is introduced in the output as a function of input X-ray energy and the second observation is degradation of the readout noise. The authors suggest that one of causes is the capacitive coupling between the BPW and the trigger signal line in the circuit layer.

In order to solve the problem, we adopt a Double-SOI wafer (DSOI) in which we introduce an additional silicon layer (a middle silicon layer) between the circuit and sensor layers. The BOX layer is interleaved with the middle silicon layer [6–8]. We expect the middle silicon layer to act as an electrostatic shield and to reduce the capacitive coupling between the BPW and the trigger signal line. In this paper, we report the first experimental results from a DSOI type of XRPIXs.

2. Device description

XRPIX3-DSOI is the first device of XRPIX using a DSOI wafer supplied by SOITEC. The devices were fabricated using the 0.2 μm fully depleted SOI CMOS pixel process by Lapis semiconductor Co., Ltd. The detector is 2.9 mm × 2.9 mm in size and consists of 32 × 32 pixels. The pixel size and the imaging area are 30 μm × 30 μm and approximately 1.0 mm × 1.0 mm, respectively. We adopted a BPW size of 14 μm in order to ensure sufficient charge-collection efficiency (CCE) [9,10]. The XRPIX3-DSOI uses the Czochralski wafer for the sensor layer with a thickness of 260 μm. Fig. 1 is the cross-sectional view of the XRPIX3-DSOI. The thickness of the middle silicon layer is 88 nm. The middle silicon layer is installed between the BOX layers. A voltage is applied to the middle silicon voltage through a via in each pixel. Both BOX layers have a thickness of 145 nm. The chip contains two test elementary groups (TEGs) of charge sensitive amplifiers (CSAs) and source followers (SFs) which are almost the same as those used in XRPIX3b reported by Takeda et al. [11]. We use SFs TEG pixels in this paper.

3. The gain as a function of the middle silicon voltage

If the output gain depends only on the parasitic capacitance between the BPW and the middle silicon layer, the output gain is predicted to be 3.1 μV/e⁻ based on the pixel layout. Actual gain should be lower than 3.1 μV/e⁻ because of other parasitic capacitance.

We obtained the spectra of X-rays from ^{241}Am with XRPIX3-DSOI in order to investigate the output gain. In the measurement, we cooled the device to −60°C in order to reduce leakage currents

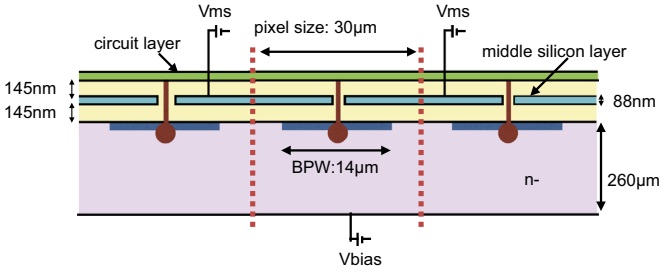


Fig. 1. Cross-sectional view of the XRPIX3-DSOI.

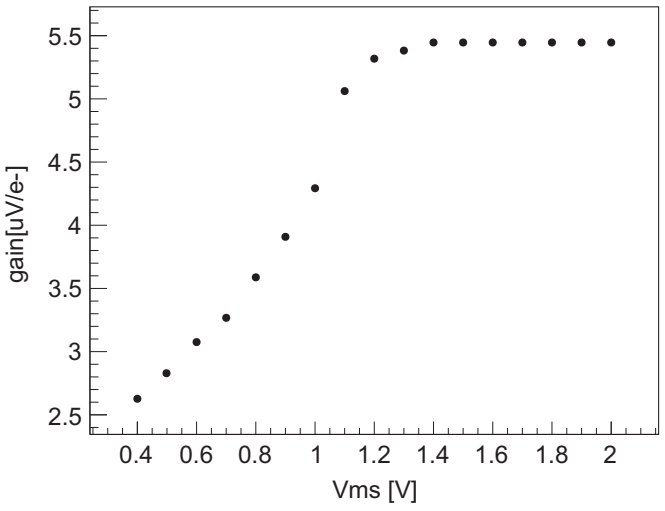
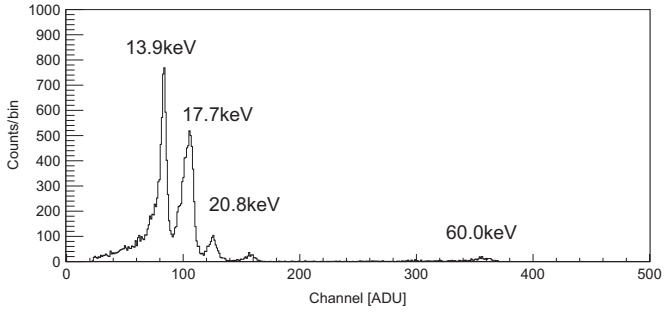


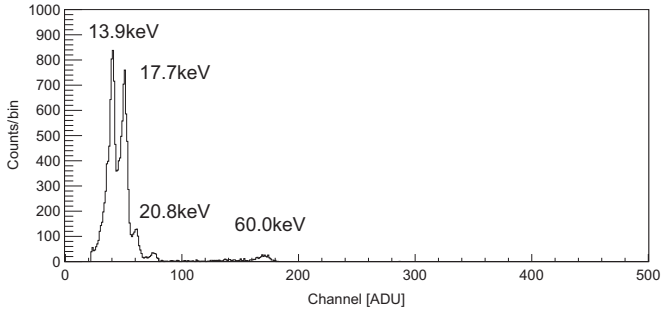
Fig. 2. Relation between the gain and the V_{ms}.

and applied a back-bias voltage of 60 V to the sensor layer. We operated it in the frame-readout mode in which we read out pulse height from all the pixels after every 1-ms exposure. We fixed the threshold of the comparator circuits (V_{th}) at a voltage corresponding to an X-ray energy of 300 keV so that the comparator circuits did not output triggers. We made spectral analyses following the method given by Ryu et al. [12].

Fig. 2 shows the output gain as a function of the middle silicon voltage (V_{ms}). Fig. 3 shows examples of spectra we obtained with V_{ms} set to 2.0 V (a) and 0.4 V (b). We note that applying too low voltage to the middle silicon layer induces an inversion layer in the sensor layer. The inversion layer electrically connects adjacent BPWs (i.e., adjacent sense-nodes), and thus the device no longer works as an imaging sensor. Therefore, the measurement started at V_{ms} of 0.4 V, which is the lowest voltage not to form the



(a) Vms=2V



(b) Vms=0.4V

Fig. 3. Spectra of ^{241}Am X-ray with V_{th} fixed at a voltage corresponding to an X-ray energy of 300 keV, hence the trigger signal is disabled. (a) V_{ms}=2 V and (b) V_{ms} =0.4 V.