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Status of the CMS Phase I pixel detector upgrade

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ABSTRACT

A new pixel detector for the CMS experiment is being built, owing to the instantaneous luminosities anticipated for the Phase I Upgrade of the LHC. The new CMS pixel detector provides four-hit tracking while featuring a significantly reduced material budget as well as new cooling and powering schemes. A new front-end readout chip mitigates buffering and bandwidth limitations, and comprises a low-threshold comparator. These improvements allow the new pixel detector to sustain and improve the efficiency of the current pixel tracker at the increased requirements imposed by high luminosities and pile-up. This contribution gives an overview of the design of the upgraded pixel detector and the status of the upgrade project, and presents test beam performance measurements of the production readout chip.

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1. Introduction

The present CMS pixel detector is a hybrid silicon pixel detector and constitutes the innermost component of the CMS tracking system [1,2]. With 66 million readout channels distributed over three barrel layers and two disk layers on either side, it is the experiment's crucial component for the primary and secondary vertex location, b-tagging, and event selection in the high-level trigger. It has been designed for an instantaneous luminosity of $\mathcal{L}=1\times 10^{34}$ cm $^{-2}$ s $^{-1}$ and performs well under these conditions with single hit efficiencies above 99.5%, and a primary vertex resolution of around 20 μm for minimum bias events with more than 50 tracks [3].

However, based on the strong performance of the LHC accelerator, it is anticipated that peak luminosities of two times the design luminosity are likely to be reached before 2018 and probably significantly exceeded in the so-called Phase I period until 2022. At this higher luminosity and increased hit occupancies the current CMS pixel detector would be subject to severe dead time and inefficiencies introduced by limited buffers in the analog readout chip and effects of increased radiation damage in the sensors.

Therefore a new pixel detector is being built and will replace the current detector in the extended year-end technical stop in 2016.

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2. The Phase I pixel detector

The main objective of the new CMS pixel detector is the maintenance and improvement of the physics performance at higher instantaneous luminosities and around 50 simultaneous inelastic collisions per bunch crossing (pile-up) [4]. The increased occupancy at these conditions necessitates new front-end electronics.

Constraints for the new detector are the existing mechanical envelope of the present system as well as the services from the detector patch panel outwards. In order to operate the new pixel detector, a new powering scheme and faster data links are required.

The tracking performance is improved by providing four barrel and three disk layers for tracking, and by significantly reducing the overall material budget of the detector. The exchange is foreseen for the extended year-end shutdown of the LHC 2016/2017.

Detector geometry and services: A new beam pipe with an outer diameter of 45 mm has been installed during the first long shutdown of the LHC. This facilitates the relocation of the innermost pixel layer closer to the interaction point, yielding an improved vertex resolution. The fourth barrel layer bridges the present gap between the outermost pixel layer and the first layer of the strip tracker, and thus reduces the track extrapolation uncertainty. The geometries of the present detector and the Phase I pixel detector are compared in Fig. 1. The z axis points along the LHC proton beam, r denotes the radial distance of the barrel layers from the z axis and θ is the polar angle. The pseudorapidity is usually favored over the polar angle, and is defined as $\eta = -\ln \tan \theta/2$.

With four barrel layers and 2×3 disks, 4-hit coverage up to pseudorapidities of $|\eta| < 2.5$ and a more robust 3-of-4 hit seeding for track candidates is possible. The total number of channels is

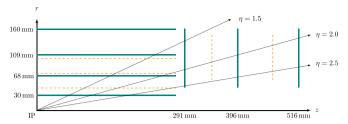


Fig. 1. Geometry of the Phase I barrel and forward pixel detectors. Shown is one quadrant of the detector, the layer radii and disk positions are given relative to the interaction point (IP). Dashed lines indicate the layer positions of the present pixel detector. © 2016 Simon Spannagel. All Rights Reserved.

almost doubled by the additional detector layers. The barrel detector granularity increases from about 48 million channels to 79 million channels, while the new forward detector features 45 million channels instead of 18 million for the present detector.

Several measures have been introduced to reduce the amount of material present in the tracking volume as indicated in Fig. 2. A reduced mass produces less photon conversions and multiple scattering from charged particles, and thus yields a better vertex resolution. A new lightweight support structure made of carbon fiber and graphite compounds reduces the material budget of the mechanical structure, while the 2-phase $\rm CO_2$ cooling system allows to operate the detector at $T=-20~\rm ^{\circ}C$ and further reduces the material due to the low coolant mass and the smaller cooling pipes with $d=1.6~\rm mm$. The most significant reduction in material is achieved by relocating many of the service electronics further down on the supply structures, out of the tracking volume. Together, these changes allow to reduce the total mass despite the additional detector layers.

Owing to constraints on the service interface, existing power supply cables have to be re-used for the operation of a significantly larger detector with its accompanying increased power consumption. Radiation-hard DC-DC converters have been developed [5], which allow to provide higher voltages over the service cables, and produce the analog and digital supply voltages for the sensors and front-end electronics close to the detector.

Sensors, front-end electronics, and readout: The sensor design remains unchanged with respect to the present pixel detector. The 285 μ m thick n⁺-in-n silicon sensors with either p-spray (barrel) or p-stop isolation (forward) feature a pixel pitch of 150 μ m \times 100 μ m in $r\phi$ and η , respectively. In addition to the pixel implants,

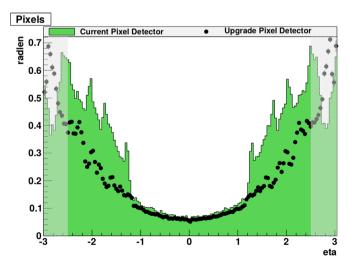


Fig. 2. The material budget of the current (shaded area) and the Phase I (black dots) pixel detector in units of radiation length as a function of the pseudorapidity η [4].

a biasing grid allows for quality tests of the sensors before being connected to the readout chip (ROC), and is shown in Fig. 3.

The connection to the ROC is established via bump bonds with a diameter of about 25 μm . The ROC is fabricated in a radiation-hard 250 nm analog CMOS technology and presents an advancement of present front-end chip design. Increased buffers have been integrated in order to mitigate data loss at high occupancies, and a global readout buffer stage allows to reduce the detector dead time. A faster pixel-cell comparator facilitates in-time thresholds as low as 1.5 ke, and the 8 bit on-chip ADC enables digital data transmission at 160 Mbit s $^{-1}$, doubling the effective bandwidth. A dedicated ROC for the innermost layer is still under design and will comprise a faster pixel readout to further reduce dead time.

The module constitutes the smallest, electrically independent unit of the pixel detector and comprises one sensor and 16 ROCs as well as the high-density interconnect (HDI) and the token bit manager (TBM). The HDI is a low-material flex print interconnect which is glued onto the sensor backplane, and houses the TBM as well as the routing for data, powering, and trigger signals. The TBM is responsible for the trigger and token control, and coordinates the readout from the ROCs. All ROC data are collected by the TBM and transmitted to the receivers outside the experiment at a bandwidth of 400 Mbit s $^{-1}$. Silicon-nitrite base-strips provide cooling contact and allow fixture of the modules to the mechanical support structure.

3. Test beam qualification of the ROC

Comprehensive test beam studies for the ROC have been performed at the DESY test beam facility. The DESY-II synchrotron accelerates positrons up to an energy of 6.3 GeV at a frequency of 1.024 MHz. This primary beam is converted via bremsstrahlung and pair production into the final test beams with 5% momentum spread at rates of a few kHz. Reference tracks are provided by the DATURA beam telescope featuring six planes with MIMOSA26 sensors [7] with an intrinsic resolution of 3.4 μm and an integration time of 120 μs . Track fitting is performed with the General Broken Lines algorithm [8,9], and track uncertainties at the device under test of about 2.5 μm can be achieved even at the comparatively low beam energies provided by the DESY-II synchrotron.

Charge collection and tracking efficiency: The charge collection behavior and tracking efficiency of the ROC have been measured as a function of the track impact point within single pixel cells. Fig. 4 shows the collected charge as a function of the track impact position for vertical track incidence. Shown is an array of 2×2 pixel cells with the x and y coordinates denoting the row direction (150 μ m pitch) and the column direction (100 μ m pitch) of the ROC, respectively. In order to increase statistics, all tracks from the ROC have been folded into the four pixel cells (Modulo 300 μ m and 200 μ m).

The bias dot is clearly visible due to the altered electric field beneath and the thus changed charge collection behavior. The structure accounts for a charge loss of about 30%.

However, owing to the 3.8 T magnetic field in the CMS tracker volume, charges drift through the silicon sensor at an angle of about 20°. This so-called Lorentz angle depends on the applied bias voltage as well as on the radiation damage, and ensures charge sharing between pixel cells. Thus, a more realistic situation is depicted in Fig. 5, where the track incidence angle is chosen to be 21°. The charge deficiency caused by the biasing grid structure is now smeared out and reduced in magnitude to about 10%.

The tracking efficiency as a function of the track impact point at vertical incidence is shown in Fig. 6, again representing four pixel cells. The tracking efficiency is defined as the fraction of reference

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