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A novel source–drain follower for monolithic active pixel sensors

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ABSTRACT

Monolithic active pixel sensors (MAPS) receive interest in tracking applications in high energy physics as they integrate sensor and readout electronics in one silicon die with potential for lower material budget and cost, and better performance. Source followers (SFs) are widely used for MAPS readout: they increase charge conversion gain $1/C_{eff}$ or decrease the effective sensing node capacitance C_{eff} because the follower action compensates part of the input capacitance. Charge conversion gain is critical for analog power consumption and therefore for material budget in tracking applications, and also has direct system impact. This paper presents a novel source–drain follower (SDF), where both source and drain follow the gate potential improving charge conversion gain. For the inner tracking system (ITS) upgrade of the ALICE experiment at CERN, low material budget is a primary requirement. The SDF circuit was studied as part of the effort to optimize the effective capacitance of the sensing node. The collection electrode, input transistor and routing metal all contribute to C_{eff}. Reverse sensor bias reduces the collection electrode capacitance. The novel SDF circuit eliminates the contribution of the input transistor to C_{eff}, reduces the routing contribution if additional shielding is introduced, provides a way to estimate the capacitance of the sensor itself, and has a voltage gain closer to unity than the standard SF. The SDF circuit has a somewhat larger area with a somewhat smaller bandwidth, but this is acceptable in most cases.

A test chip, manufactured in a 180 nm CMOS image sensor process, implements small prototype pixel matrices in different flavors to compare the standard SF to the novel SF and to the novel SF with additional shielding. The effective sensing node capacitance was measured using a ^{55}Fe source. Increasing reverse substrate bias from -1 V to -6 V reduces C_{eff} by 38% and the equivalent noise charge (ENC) by 22% for the standard SF. The SDF provides a further 9% improvement for C_{eff} and 25% for ENC. The SDF circuit with additional shielding provides 18% improvement for C_{eff}, and combined with -6 V reverse bias yields almost a factor 2.

1. Introduction

A monolithic active pixel sensor [1] integrating sensors and readout circuitry into the same silicon chip will equip the new inner tracking system (ITS) of the ALICE experiment after the second long shutdown of the LHC in 2019 [2–4]. The advantages of MAPS are low production cost, easy assembly, and good power – signal-to-noise ratio performance. The TowerJazz 180 nm CMOS image sensor process with high resistivity epitaxial layer ($\rho > 1$ kΩ cm) has been chosen for the prototype implementation [5]. Fig. 1 shows the sensor cross-section. A special feature of this technology is the deep p-well underneath the PMOS n-well, that prevents it from competing in charge collection with the designated collection electrode. Therefore, full CMOS circuits can be

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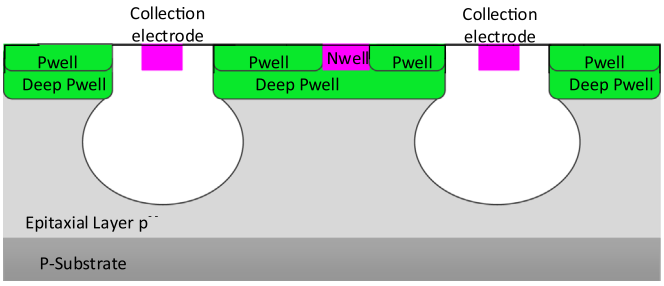

Fig. 1. Sensor cross-section.

implemented in the pixel, significantly widening the possibilities for the readout circuit. The charge collection diode is the n-well – p^{--} epitaxial layer junction. Low material budget is a primary requirement for the ITS upgrade. Indeed a low power consumption could significantly reduce the material budget for power cables and cooling system. The analog power consumption is determined by the required S/N ratio for a given bandwidth [6]:

$$P \propto \left\{ \frac{S/N}{Q/C_{eff}} \right\}^m, \quad 2 \le m \le 4 \tag{1}$$

where P is the power consumption, Q is the collected charge, and C_{eff} is the effective sensing node capacitance. For this reason a low value of sensing node capacitance allows for power reduction.

The source follower (SF) circuit is traditionally used to read out the sensing node voltage signal. The SF circuit compensates part of the sensing node capacitance because of the follower action. In the past years, some variants of the conventional SF have been developed. A low output resistance super SF is analyzed in [7]. A low-distortion broad-band cascade-complementary SF is analyzed in [8]. An enhanced slew-rate SF is analyzed in [9]. The novel source drain follower (SDF) circuit presented in this paper accomplishes a larger reduction of the sensing node capacitance by removing also the contribution of the input transistor and metal routing. Therefore the SDF circuit can also be used for a direct measurement of the sensor capacitance. In the following the novel SDF circuit model with implementation details and prototype measurement results are reported.

2. Standard source follower

The standard source follower is shown in Fig. 2. The small signal model is analyzed in [7]. The PMOS transistor M_1 bulk is tied to the source, hence the body effect can be ignored in the DC voltage gain calculation. M2 can be sized such that $r_{o2} \gg r_{o1}$. The DC gain can therefore be expressed as:

$$A_{v_{SF}} = \frac{g_{m1} r_{o1}}{1 + g_{m1} r_{o1}} \tag{2}$$

where the input transistor M_1 intrinsic gain $g_{m1} r_{o1} \gg 1$, and therefore $A_{v_{SF}} \to 1$. The gate-source capacitance of the input transistor M_1, namely C_f, is not charged because the difference between gate and source voltage is constant. Hence the effective sensing node capacitance is:

$$C_{eff_{SF}} = C_d + C_p + C_{gd} \tag{3}$$

where C_d is the detector capacitance, C_p is the input routing metal capacitance, and C_{gd} is the gate to drain capacitance.

The frequency content of signals in MAPS as they are collected is larger than 10 MHz. The $1/f$ noise corner frequency f_C depends on the transistor size and drain current. In deep submicron CMOS processes, the f_C for a minimum size PMOS transistor with low

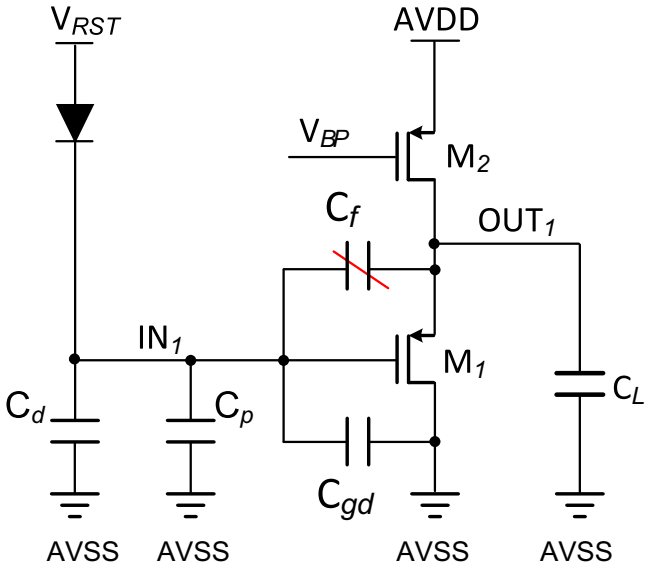

Fig. 2. Standard source follower with the diode reset and parasitic capacitances. The back slash across the capacitor C_f indicates that it does not need to be charged by the input charge.

drain current is well below 100 kHz. In this process the f_C was simulated to increase monotonically up to 50 kHz at 1 μA bias current for the minimum size of $W/L = 0.22\ \mu m/0.18\ \mu m$, and to be almost independent of width for constant current density. If the signals are treated in real time, $1/f$ noise sources can be neglected, and only thermal noise is taken into account in noise calculations. If the signal is stored on the input node for a longer time, $1/f$ noise can become more important, but then one of the advantages of the SDF circuit which will be discussed in Section 3 is that the size of the input transistor can be increased to reduce its $1/f$ noise contribution without penalty on the input capacitance as the contribution of the input transistor to the effective input capacitance is eliminated. Therefore we have neglected the $1/f$ noise in the noise analysis. The SF circuit noise is calculated assuming two thermal noise voltage sources $N_1 = \sqrt{4kT\gamma/g_{m1}}$ and $N_2 = \sqrt{4kT\gamma/g_{m2}}$ on M_1 and M_2 gates as shown in Fig. 3(a). The equivalent small-signal model circuit is shown in Fig. 3(b). Using Kirchhoff's voltage Law (KVL) and Kirchhoff's current Law (KCL), we obtain:

$$V_{g1} = N_1 + \frac{C_f}{C_f + C_{eff}} V_{n,o} \tag{4}$$

$$-V_{n,o} \frac{C_f C_{eff}}{C_f + C_{eff}} s - g_{m1}(V_{n,o} - V_{g1}) + g_{m2} N_2 - V_{n,o} s C_L = 0. \tag{5}$$

Rearranging Eqs. (4) and (5), the voltage noise spectral density is:

$$V_{n,o}(f) = \frac{C_{eff} + C_f}{C_{eff}} (N_1 + \frac{g_{m2}}{g_{m1}} N_2) \frac{1}{1 + 2\pi f \frac{C_L C_f + C_{eff} C_L + C_{eff} C_f}{g_{m1} C_{eff}} i}. \tag{6}$$

Considering the case of the thermal noise in weak inversion region and $g_{m1} = g_{m2}$, and assuming $\gamma = 1/2$ for this case, the root mean square of the noise voltage is:

$$V_{rms,no} = \sqrt{\int_0^\infty V_{n,o}^2 \, df} = \sqrt{kT \frac{(C_f + C_{eff})^2}{C_{eff}(C_L C_f + C_{eff} C_L + C_{eff} C_f)}} \tag{7}$$

where k is the Boltzmann constant and T is the absolute temperature. Under the assumption of a unity gain SF circuit, the equivalent noise charge (ENC) expression is:

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