Nuclear Instruments and Methods in Physics Research A 830 (2016) 119–129

Contents lists available at ScienceDirect

Nuclear Instruments and Methods in Physics Research A

journal homepage: www.elsevier.com/locate/nima

# A silicon photo-multiplier signal readout using strip-line and waveform sampling for Positron Emission Tomography

H. Kim [a,*], C.-T. Chen [a], N. Eclov [a], A. Ronzhin [b], P. Murat [b], E. Ramberg [b], S. Los [b], C.-M. Kao [a]

[a] Department of Radiology, University of Chicago, Chicago, IL 60637, USA
[b] Fermi National Accelerator Laboratory, IL, USA

ARTICLE INFO

*Article history:*
Received 31 January 2016
Received in revised form
15 May 2016
Accepted 22 May 2016
Available online 24 May 2016

*Keywords:*
Positron Emission Tomography
Strip-Line Readout
Waveform Sampling
Multiplexing

ABSTRACT

A strip-line and waveform sampling based readout is a signal multiplexing method that can efficiently reduce the readout channels while fully exploiting the fast time characteristics of photo-detectors such as the SiPM. We have applied this readout method for SiPM-based time-of-flight (TOF) positron emission tomography (PET) detectors. We have prototyped strip-line boards in which 8 SiPMs (pitch 5.2 mm) are connected by using a single strip-line, and the signals appearing at the ends of the strip-line are acquired by using the DRS4 waveform sampler at a nominal sampling frequency of 1–5 GS/s. Experimental tests using laser and LYSO scintillator are carried out to assess the performance of the strip-line board. Each SiPM position, which is inferred from the arrival time difference of the two signals at the ends of the strip-line, is well identified with 2.6 mm FWHM resolution when the SiPMs are coupled to LYSO crystals and irradiated by a $^{22}$Na source. The average energy and coincidence time resolution corresponding to 511 keV photons are measured to be ~32% and ~510 ps FWHM, respectively, at a 5.0 GS/s DRS4 sampling rate. The results show that the sampling rate can be lowered to 1.5 GS/s without performance degradation. These encouraging initial test results indicate that the strip-line and waveform sampling readout method is applicable for SiPM-based TOF PET development.



## 1. Introduction

The silicon photo-multiplier (SiPM) [1–4] is an attractive photosensor for developing time-of-flight Positron Emission Tomography (TOF PET) scanner. It is considered to be a substitute for the vacuum-based photo-multiplier tube (PMT). Its advantageous features include high electrical gain comparable to the conventional PMT, fast time response, and in-sensitiveness to magnetic fields. In addition, the compact size of SiPMs makes it possible to couple scintillators to photo-detectors individually, thereby allowing flexible detector designs to achieve high spatial resolution or to increase the sensitivity [5]. On the other hand, SiPMs show a high dark count rate (~1 MHz/mm$^2$) and are sensitive to temperature and voltage variations [6,7]. Since the typical effective area of the SiPMs currently available in the market is $\sim 1\times 1 - 6\times 6$ mm$^2$, a clinical PET scanner can use several thousands or more SiPMs. The signal readout of such a large number of SiPMs would be a challenge; for example, our brain PET design [8], with a diameter of 240 mm and an axial field-of-view (FOV) of 40 mm, requires 1152 SiPMs, assuming each SiPM pixel is $5\times 5$ mm$^2$ in size.

The charge division resistor network is a popular multiplexing readout method for SiPMs. In this method, outputs of SiPMs in an array, e.g., $4\times 4$ or $8\times 8$, are interconnected with resistors, and the position of the signal initiating SiPM in the array is calculated from the relative amount of charges measured at 4 corners of the resistor network. Although this method could achieve a large multiplexing ratio, the large capacitance of a SiPM coupled to resistors causes a long rise time of the output signal; therefore, it is not adequate for TOF PET applications. However, the method is commonly adopted by small animal PET systems because they do not need TOF ability. Some implementations based on the method have been reported in [9–12], and a comprehensive review on signal multiplexing for SiPMs is found in [13].

We have developed a signal multiplexing method based on strip-line readout that can keep the fast time characteristic of the SiPM. Initially, we developed the method to efficiently handle signals from large area micro-channel plate PMTs [14,15]. In this approach, the micro-channel plate PMT signals are collected by anode strips placed in parallel across the photo-detector area. The signals on the strip-line propagate to both ends of the strip, and are digitized by using a high speed waveform sampler, e.g., a Domino Ring Sampler (DRS) [16]. The event information, including the energy and time of the gamma interaction, are obtained by processing the digitized waveform, and the position of the

* Corresponding author.
*E-mail address:* heejongkim@uchicago.edu (H. Kim).

http://dx.doi.org/10.1016/j.nima.2016.05.085
0168-9002/

interaction is inferred from the difference in time when the signals arrive at the ends of the strip-line (called the differential time, or dT, below). This method is applicable to SiPM as well; therefore, we have prototyped strip-line boards for SiPMs and demonstrated the feasibility of the strip-line readout in a previous paper [17,18]. Based on these early experiences, we have built second-generation strip-line boards intended for our brain PET system development. Another important feature of our readout is the use of waveform sampling [19] to ensure precise time measurement and fully exploit the fast time characteristics of the SiPMs. Using the DRS4 chip, we have developed a PDRS4 waveform sampling board [20] that provides a high channel density, an adjustable sampling rate, and adequate memory depth for PET applications. Experimental tests have been carried out using pulsed laser and Lutetium-Yttrium OxyorthoSilicate (LYSO) scintillator to characterize the performance of this strip-line and waveform sampling readout. The sampling rate of the DRS4 was varied to assess how the sampling rate affects the detector performance.

The remainder of this paper is organized as follows. In Section 2, we explain the development of the strip-line board and PDRS4 waveform sampling board. The experimental test setup is also described. The test results using laser and LYSO scintillator are presented in Section 3. Discussion and summary are given in Sections 4 and 5, respectively.

## 2. Materials and methods

### 2.1. Strip-line boards

The strip-line board (SLB) has four strip-lines laid out in $8 \times 3$ cm$^2$ FR4 substrate, and eight SiPMs in a row are connected by a strip-line. Currently, only two strip-lines in each board are installed with 16 (8 SiPMs on each strip-line) SPM42–75 SiPMs (STM, Italy) [21,22]. Each SiPM has 3342 micro-pixels in a $4.0 \times 4.4$ mm$^2$ active area with a 54% fill factor. The pitch between SiPMs is 5.2 mm. All SiPMs on the board are biased to the same voltage of –31.5 V. The nominal breakdown voltage of the SiPMs is about –28 V. Fig. 1(a) shows a photo of the strip-line board in which the SiPMs on the top row are individually coupled to LYSO crystals. Fig. 1(b) depicts SiPM numbering on a strip-line and PDRS4 readout channel assignment adopted in this paper. To decouple the capacitance of the SiPM and hence maintain the fast timing characteristics [23], a common base buffer transistor (2SC5662, ROHM Semiconductor) is used between the SiPM and strip-line as depicted in Fig. 1(c). With this decoupling scheme, the low input impedance of a common base buffer minimizes response time of the SiPM, while low capacitance and high impedance of the output minimize strip-line performance degradation and provide separation between SiPMs on a strip-line. The details of the circuit implementation of the board are described in [17]. In this study, two strip-line boards are used. One is configured with a 0.6 V strip-line bias (SLB#2), while the other uses a 0 V (SLB#1). The idea is to see whether the simplified biasing (0 V) can perform as well as the other. The use of different biases results in different transistor output capacitances (Fig. 1(d)); therefore, the SiPM signals on the two SLBs will show different amplitude and rise time behaviors. When using the leading-edge discrimination with a fixed threshold for time measurement, the different signal shapes will result in an apparent difference in the signal propagation time on the strip-line board.

### 2.2. Waveform sampling by PDRS4

The waveforms of the strip-line board signals are acquired by using the PDRS4 board [20] developed by us and NOTICE. The PDRS4 board, shown in Fig. 2(a), uses a DRS4 sampling chip [16], which is based on switched capacitor array technology. The board provides 8 input channels, each having a 1024 buffer depth, and the nominal sampling rate is adjustable between 0.7 and 5.0 giga-samples per second (GS/s). In the PDRS4 board, the capacitor voltages of the DRS4 are digitized by using a 12 bit octal Analog to Digital Converter (ADC) (AD9222, Analog Devices), and the digitized waveforms can be transferred through 100 Base-T Ethernet or a small form-factor pluggable transceiver to a data acquisition computer. The ground levels of the 8 input channels of the PDRS4 are adjustable by setting a 12 bit Digital to Analog Converter (DAC) (TLV5630IPW, Texas Instruments); in this work, the DAC values of all channels are set to 500 because the SiPM output signals have a positive polarity. The amplitude offset and gain variation of the 1024 capacitor cells in the DRS4 chip are measured by acquiring data with DC input signals, as described in [20]. Fig. 2(b) shows a PDRS4 waveform of the DC input before and after the offset of each capacitor cell in the DRS4 is corrected by using the measured value. From the waveform after the offset correction, the PDRS4 noise level is measured to be ~6.1 ADC counts, shown in Fig. 2(c), which is equivalent to ~1.5 mV [20]. The sampling interval between adjacent DRS4 sampled points is not uniform and needs to be measured individually for precise time measurement. The non-

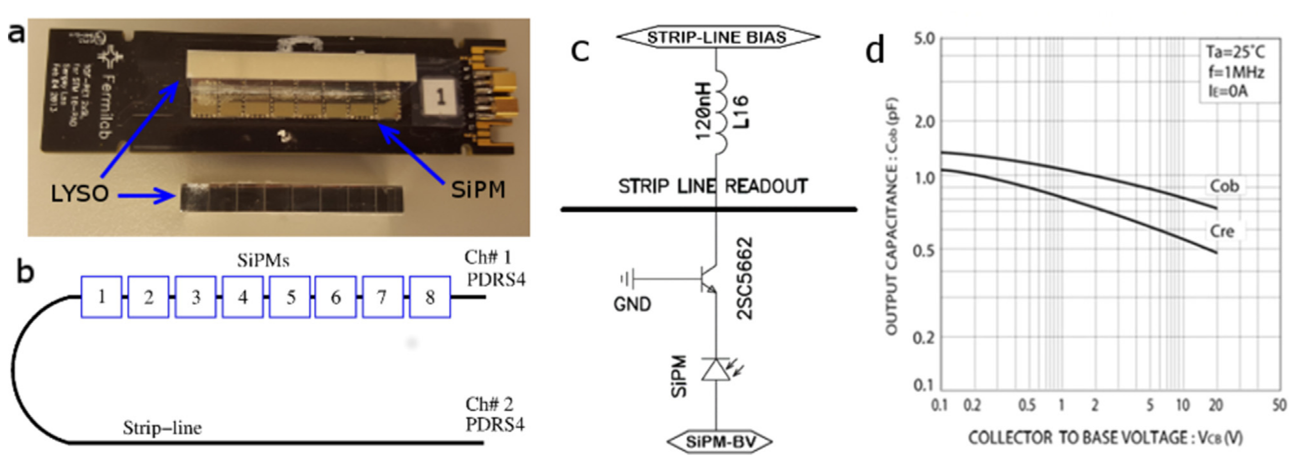


**Fig. 1.** (a) A strip-line board (SLB#1). A linear array of eight LYSO scintillators is coupled to 8 SiPMs on a strip-line on the board. (b) The numbering of SiPMs on a strip-line and PDRS4 readout channel assignment. (c) A schematic diagram shows the biasing scheme for a buffer transistor (ROHM 2SC5662). Two strip-line boards are used in this work and the strip-line bias is 0 V for SLB#1 and 0.6 V for SLB#2. (d) The output capacitance vs. bias voltage for the 2SC5662 transistor across the collector and base [24].