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Investigation of HV/HR-CMOS technology for the ATLAS Phase-II Strip Tracker Upgrade

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ABSTRACT

ATLAS has formed strip CMOS project to study the use of CMOS MAPS devices as silicon strip sensors for the Phase-II Strip Tracker Upgrade. This choice of sensors promises several advantages over the conventional baseline design, such as better resolution, less material in the tracking volume, and faster construction speed. At the same time, many design features of the sensors are driven by the requirement of minimizing the impact on the rest of the detector. Hence the target devices feature long pixels which are grouped to form a virtual strip with binary-encoded z position. The key performance aspects are radiation hardness compatibility with HL-LHC environment, as well as extraction of the full hit position with full-reticle readout architecture. To date, several test chips have been submitted using two different CMOS technologies. The AMS 350 nm is a high voltage CMOS process (HV-CMOS), that features the sensor bias of up to 120 V. The TowerJazz 180 nm high resistivity CMOS process (HR-CMOS) uses a high resistivity epitaxial layer to provide the depletion region on top of the substrate. We have evaluated passive pixel performance, and charge collection projections. The results strongly support the radiation tolerance of these devices to radiation dose of the HL-LHC in the strip tracker

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region. We also describe design features for the next chip submission that are motivated by our technology evaluation.

1. Introduction

Traditional silicon tracking systems in High-Energy Physics feature heterogeneous architecture of separately produced sensors and readout amplifier chips. As a consequence, their interconnect becomes a significant aspect of the system integration when the number of readout channels is in the range of 10 s and 100 s of million. Attempts to make monolithic sensors have been long made. One interesting example is HV-CMOS technology [1]. It attracted significant attention due to recent indications of its radiation hardness [2,3].

The indications instigated ATLAS to investigate this technology for its suitability for the upgraded strip tracker (there is a similar program for pixel system [4]). The sensor design has to be pixelated to limit the amplifier's input capacitance and therefore noise. The consequence of this is a potential of reducing the active surface area by about a factor of two compared to the traditional design of two strip layers giving one 3D hit position using a small crossing angle [5]. An additional benefit is a better positional resolution. With less active area in the same volume, the tracker will have less radiation length. There is also a potential for shorter construction time, and reduced sensor cost.

In order to have a practical possibility of implementing the CMOS sensors for ATLAS Phase-II Tracker Upgrade, the design changes to the rest of the tracker have to be minimal. Therefore, the program aims at preserving the baseline architecture of staves and petals composed of modules, which in turn are composed of sensors and hybrids. The big difference compared to the baseline design is that a) the sensors have built-in amplifiers, b) the sensors have comparators and fast hit encoding engine in the peripheral region, c) the readout chips have only digital circuitry. The readout chips would still contain digital pipeline, trigger and command interfaces. They would be a simplified version of the current prototype chips. Due to the hit encoding in the sensors, the information exchange between the sensors and readout chips can be implemented on a fast digital bus, which uses far fewer wirebonds than the traditional scheme of 1 bond per channel.

While the CMOS sensors have a potential to bring in these attractive performance features, the key issue is their performance and radiation hardness for doses relevant for the strip region: 60 Mrad and 2×10^{15} neq/cm^2 [5]. The first year of the evaluation program aims at characterizing the basic properties of the technology. We chose two foundries for this evaluation. One is HV-CMOS process from AMS with 350 nm feature size. It features a possibility of biasing the substrate of up to 120 V to provide a thin depletion region. The second process is HR-CMOS 180 nm from TowerJazz. It implements a high resistivity epitaxial layer on top of a substrate that can be used as a charge collection medium.

At the time of this writing we have results from AMS HV-CMOS process. We give their overview in this paper, with an emphasis on passive pixel tests. They are an important part of the monolithic sensor design, defining the signal level, influencing the attainable noise and spatial accuracy of the sensor. The passive pixel tests are a new aspect of this technology investigation compared to the earlier publications [2,3].

2. Test ASICs

With both technologies chosen for our evaluation we expect the signal level to be significantly smaller than for traditional hybrid strips or pixel systems. Therefore a special attention has to be payed to both the signal and noise level achievable. In case of the TowerJazz technology the depletion region is limited to that of maximal epitaxial layer thickness, of about 25 μm. This aspect of the technology constraints the signal level one can expect to obtain. The AMS technology allows for use of higher bulk resistivities that could lead to higher signal level. This will be explored in future chip submissions (Section 4).

In order to facilitate the technology characterization, we had several test ASIC submissions. Their designs implemented test structures to enable several types of critical tests. To investigate signal-to-noise ratio and to develop design for a large scale chip, it is important to know signal level after bulk damage due to radiation. A key aspect of the noise performance is the pixel capacitance present on the amplifier input. The ASIC design toolkits cannot estimate these factors, so we included passive pixel structures to measure these parameters after irradiation.

Another key aspect of the CMOS sensors is amplifier implementation inside the pixel area, where as the comparators and digital processing are planned to be put in the sensor periphery to avoid extra noise. The finite density of signal lines running from each pixel to the periphery requires use of relatively long pixels, up to 800 μm. We included structures with varying length to study its effect on the performance.

The total of 3 test ASICs have been made to date:

- HVStripV1 chip in the HV-CMOS technology. It had test transistors, 2 rows of active pixels of 40×400 μm^2 size with discriminators and digital readout scheme, and pixel structures with analog readout.
- CHESS-1-AMS chip in the HV-CMOS technology. It contained test transistors, passive pixels of varying length, standalone amplifiers, and active pixels with embedded amplifiers (Fig. 1). The chip also contained specialized structures: a large passive array to aid charge collection studies, and a passive pixel array near the edge to allow for depletion region studies with sidewise illumination. All test structures featured design rules for 120 V bias. The fraction of pixel area occupied by the collecting n-well was varied for the passive pixels. In some test structures n-well area was 30% of the total pixel area, and in others it was 50%. The passive pixel test structure connection scheme is shown in Fig. 2.
- CHESS-1-TJ chip in the HR-CMOS technology. Similarly to CHESS-1-AMS, it contained transistors, passive pixels, standalone amplifiers, and active pixels. In addition, it had a variation of the epitaxial layer thickness and different bulk types. The collecting diode geometry was varied for passive pixels.

CHESS-1 chips had implemented a different design philosophy, consistent with prior designs in these technologies. CHESS-1-AMS had the active pixel amplifiers embedded in the collecting n-wells. CHESS-1-TJ had the circuit placed in a separate well from the small collecting diode. In principle, both design choices can be implemented in either technology. This small collected diode design can drastically minimize the amplifiers input capacitance to arrive at a lower noise level. This is important for the TowerJazz technology due to the limited signal level due to epitaxial layer thickness. However, the field geometry in the depleted region may be more complicated this case, especially after bulk damage after hadron irradiation. Therefore a special attention will have to be

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