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Radiation-hard/high-speed parallel optical links

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ABSTRACT

We have designed and fabricated a compact parallel optical engine for transmitting data at 5 Gb/s. The device consists of a 4-channel ASIC driving a VCSEL (Vertical Cavity Surface Emitting Laser) array in an optical package. The ASIC is designed using only core transistors in a 65 nm CMOS process to enhance the radiation-hardness. The ASIC contains an 8-bit DAC to control the bias and modulation currents of the individual channels in the VCSEL array. The performance of the optical engine up at 5 Gb/s is satisfactory.

1. Introduction

A parallel optical engine is a compact device for high-speed data transmission. The compact design is enabled by readily available commercial high-speed VCSEL arrays. These modern VCSELs are humidity tolerant and hence no hermitic packaging is needed [1]. With the use of a 12-channel array operating at 10 Gb/s per channel, a parallel optical engine can deliver an aggregate bandwidth of 120 Gb/s. With a standard spacing of 250 µm between VCSELs, the width of a 12-channel array is only slightly over 3 mm. This allows the fabrication of a rather compact parallel optical engine for installation in locations where space is at a premium. The use of a fiber ribbon also reduces the number of fibers to handle and moreover a fiber ribbon is less fragile than a single-channel fiber. These advantages greatly simplify the production, testing, and installation of optical links.

VCSEL arrays are widely used in off-detector data transmission in high-energy physics [2]. The first implementation [3] of VCSEL arrays for on-detector application is in the optical links of the ATLAS pixel detector. The experience from the operation of this first generation of array-based links has been quite positive. In particular, the failure rate of the optical links fabricated by The Ohio State University is ~0.1% [4]. The ATLAS experiment therefore continues to use VCSEL arrays in the second-generation optical links [5] for a new layer of the pixel detector, the insertable barrel layer (IBL), installed in early 2014 during the long shutdown (LS1) to prepare the LHC for collisions at the center-of-mass energy of 13 TeV. In addition, ATLAS also decided to move the optical links of the original pixel detector to a more accessible location. The replacement optical links are also array based.

The optical modules (optical engines or opto-boards) for the two generations of optical links for the ATLAS pixel detector are similar in design. However, there are several improvements in the second-generation opto-boards [5] to increase the reliability of the opto-board and simplify the fabrication procedure. In particular, the optical package (opto-pack) has a much more robust design [6]. About 400 opto-boards were fabricated, corresponding to about 6000 uplinks (from the pixel detector up to the counting room) and 3000 downlinks (from the counting room down to the pixel detector). The links are operated at 40–160 Mb/s.

Based on this extensive and positive experience, it is logical for the ATLAS pixel detector of the HL-LHC to continue to use optical links based the opto-board concept. In these proceedings, we report the result of an R&D project on the next generation optical engine operating at high speed.

2. Design of the opto-board

The opto-board is a miniature printed circuit board (PCB). Fig. 1 shows a drawing of the opto-board. A VCSEL array driver ASIC is mounted on the opto-board next to an opto-pack. This keeps the length of the wire bonds between the ASIC and the VCSEL array to a minimum to minimize the parasitic capacitance and inductance of the wire bonds. This allows the ASIC to drive the VCSELs at high speed. The PCB has a thick copper back plane (1.0 mm) that can be

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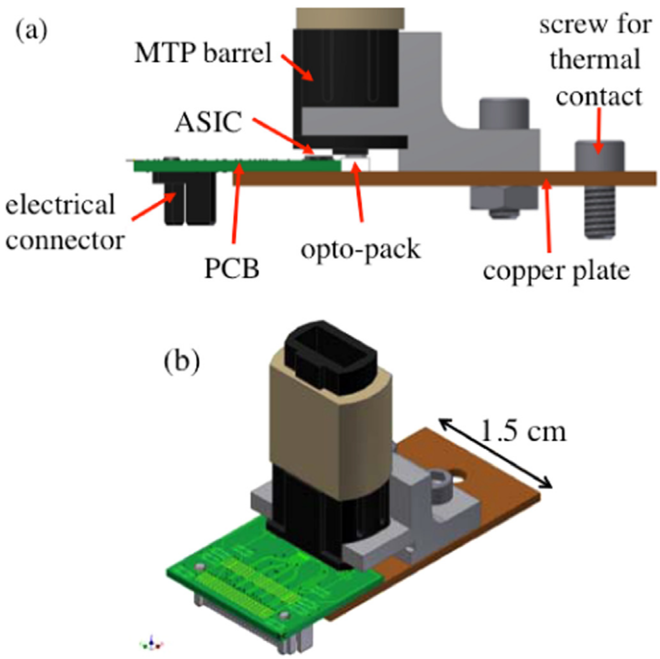

Fig. 1. (a) Schematic drawing of an opto-board together with a MTP barrel fastened to the opto-board for the insertion of a fiber ribbon terminated with MTP connector to receive the optical signal from the VCSEL array. (b) A three-dimensional rendition of above setup.

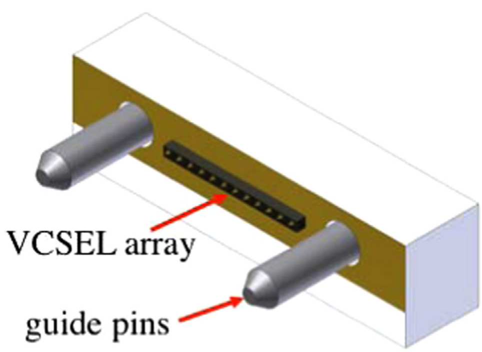

Fig. 2. Schematic drawing of an opto-pack. The distance between the two guide pins is 4.6 mm.

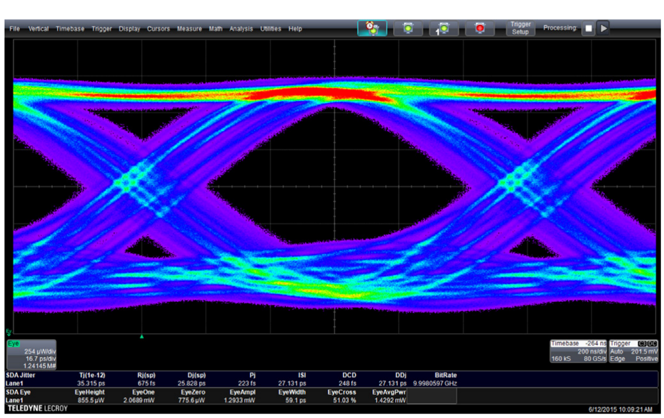

Fig. 3. Optical eye diagram of a VCSEL channel coupled to a driver ASIC operating at 10 Gb/s.

fastened with a screw to a heat sink to remove the heat generated by the ASIC and VCSEL array. The heat sink can be a copper rail with tube in the center for the passage of coolant. An MTP barrel

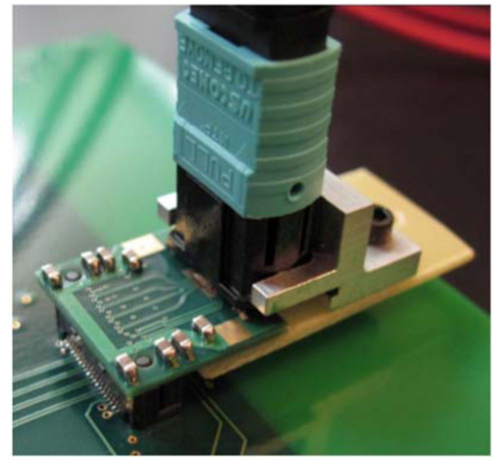

Fig. 4. Opto-board with an MTP connector attached.

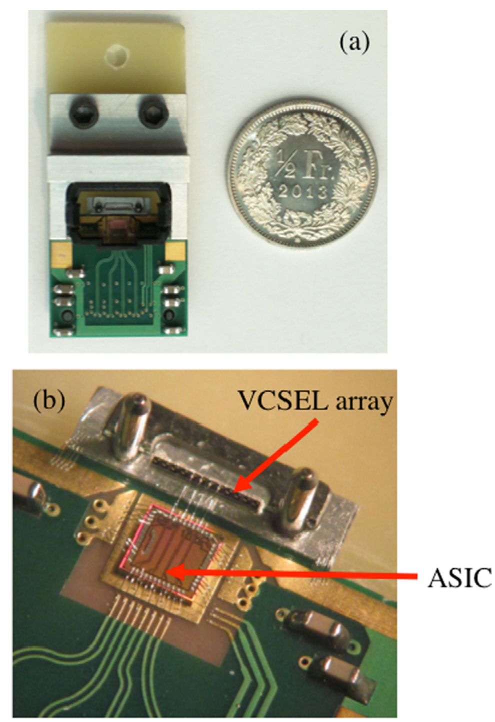

Fig. 5. (a) Top view of an opto-board. (b) A zoom-in view showing the placement of the ASIC with respect to the VCSEL array between the two guide pins on an opto-pack.

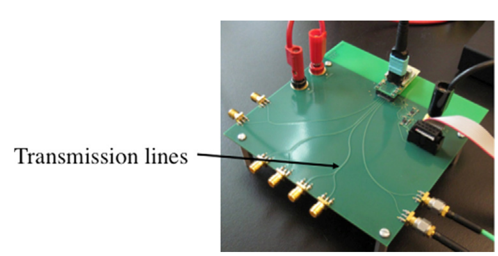

Fig. 6. An emulator of the back plane of the opto-box for sending high-speed electrical signals to the opto-board.

attached to an aluminum brace is fixed to the opto-board via a screw. A fiber ribbon terminated with a MTP connector can be inserted into the MTP barrel to receive the optical signal from the VCSEL array. The spring-loaded MTP connector is widely used in the optical communication industry due to its ease of use. An

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