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Performance of silicon pixel detectors at small track incidence angles for the ATLAS Inner Tracker upgrade

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ABSTRACT

In order to enable the ATLAS experiment to successfully track charged particles produced in high-energy collisions at the High-Luminosity Large Hadron Collider, the current ATLAS Inner Detector will be replaced by the Inner Tracker (ITk), entirely composed of silicon pixel and strip detectors. An extension of the tracking coverage of the ITk to very forward pseudorapidity values is proposed, using pixel modules placed in a long cylindrical layer around the beam pipe. The measurement of long pixel clusters, detected when charged particles cross the silicon sensor at small incidence angles, has potential to significantly improve the tracking efficiency, fake track rejection, and resolution of the ITk in the very forward region. The performance of state-of-the-art pixel modules at small track incidence angles is studied using test beam data collected at SLAC and CERN.

1. Introduction

The Large Hadron Collider (LHC) is foreseen to be upgraded in 2024–2026 to become the High-Luminosity LHC, delivering proton–proton collisions at a levelled luminosity of $7.5 \times 10^{34}\ \mathrm{cm^{-2}\ s^{-1}}$, with an average pileup of $\langle \mu \rangle = 200$ collisions every 25 ns. The ATLAS experiment [1] will need to be upgraded to successfully operate given such high collision rates. In particular, the current ATLAS Inner Detector will need to be completely replaced by a new Inner Tracker (ITk), made of silicon pixel and strip detectors.

Different design layouts for the ITk are currently being evaluated using simulated data, based on tracking performance figures of merit such as tracking efficiency, resolution, and pattern recognition capabilities. Many of these designs aim to extend the tracking coverage of the ITk to very forward pseudorapidity[4] values up to $|\eta| = 4$, in order to enable significant improvements in pileup jet suppression, vertex reconstruction, *b*-tagging, lepton identification and missing transverse momentum resolution [2]. Sensors placed parallel to the beam pipe at very forward pseudorapidity are crossed by tracks at small incidence angles.

The goal of this study is to characterize the performance of pixel detectors at incidence angles from 2° to 15° with respect to the sensor plane, using test beam data collected in 2015 at SLAC End Station A and at the CERN SPS. Following more information about the context relevant to this research in Section 2, the devices under test, experimental setup and data analysis methods are described in Section 3. Results from the SLAC and CERN test beams are presented in Sections 4 and 5 respectively.

2. Extended inner pixel barrel layers for the ITk

A possible ITk layout design currently under investigation is

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[4] ATLAS uses a right-handed coordinate system with the *z*-axis along the beam pipe. Cylindrical coordinates (r,ϕ) are used in the transverse plane. Pseudorapidity is defined in terms of the polar angle θ as $\eta = -\ln\tan(\theta/2)$.

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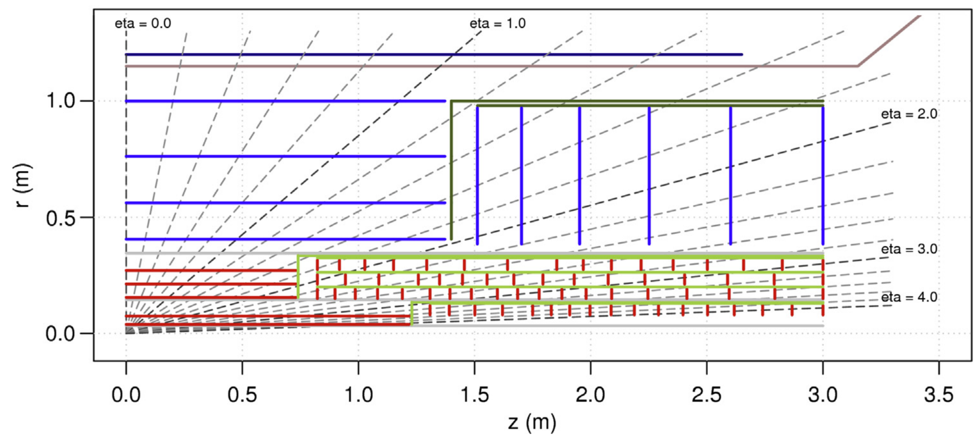

Fig. 1. Possible ITk layout design with pseudorapidity coverage up to $|\eta| = 4$. Stereo strip detector layers are shown in light blue, and the pixel detector is shown in red. A possible routing for services is shown in green. The brown line outside the ITk volume represents the cryostat boundary, and the dark blue line represents the coil of the solenoid magnet. Lines of constant pseudorapidity are shown in gray. (For interpretation of the references to color in this figure caption, the reader is referred to the web version of this paper.)

shown in Fig. 1. Hermetic coverage up to $|\eta| = 4$ is achieved by means of an extension of the two inner pixel barrel layers up to $z = 1.22$ m, accompanied by an adequate number of pixel ring layers in the forward region.

With this layout, the innermost pixel barrel layer provides a measurement as close as possible to the interaction point for the entire pseudorapidity range, resulting in expected improvements in tracking efficiency and resolution. Charged particle tracks at high pseudorapidity cross the extended pixel barrel layers at small incidence angles, giving rise to long clusters of pixel hits, as shown in Fig. 2.

Measured long clusters can be considered as short track segments, or "tracklets", since they contain directional information about the track. Explicitly, for a given sensor thickness t and pitch p, the cluster length N_{pix} provides a measurement of the track angle θ as

$$\tan\theta = \frac{t}{(N_{pix} - \delta) \times p} \quad (1)$$

where $\delta = 1$ is used to account for the difference between the measured cluster length and the distance between the track entry and exit points in the beam direction.

It is therefore possible to use long clusters as seeds during the pattern recognition phase of track reconstruction, by only considering track candidates where the pixel cluster lengths are compatible with the track angle. This is expected to result in considerable savings in computing time, as well as lower fake track rates, compared with a detector where this information is absent. Early simulation results show that the cluster length information can be used for pattern recognition as soon as the expected cluster length is greater than or equal to 3 pixels.

Pixel modules in the ITk are currently expected to have a pitch of $50\,\mu m \times 50\,\mu m$, and a sensor thickness of 100–150 μm. With a sensor thickness of 150 μm, clusters are expected to have a length of 3 pixels for tracks at $|\eta| = 0.63$, 18 pixels at $|\eta| = 2.5$ and 83 pixels at $|\eta| = 4.0$.

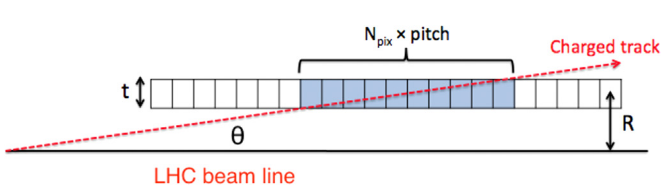

Fig. 2. Schematic of a long pixel cluster caused by the passage of a charged particle with a small track incidence angle θ.

In the absence of multiple scattering effects and without making use of pixel charge information, the resolution on the cluster length N_{pix} is limited by the pitch, in pixel units $1/\sqrt{12}$ for each of the entry and exit pixel positions, for a combined total of $1/\sqrt{6}$. Following Eq. (1), the angular resolution achieved with this technique therefore improves for smaller values of the track incidence angle θ. As will be seen, the influence of multiple scattering can be appreciated only for the smallest angle (2°), indicating that for $50\,\mu m \times 50\,\mu m$ pixels, multiple scattering does not degrade the measurement until the path length in silicon exceeds 3 mm. This is consistent with analytic calculation.

3. Experimental methods

3.1. Devices under test

Four un-irradiated pixel modules, produced for the Insertable B-Layer (IBL) [3] upgrade to the ATLAS detector, are tested: two double-chip modules with planar sensors (200 μm thick), with production numbers 93-04-03 and 94-01-04 and two single-chip modules with 3D sensors (230 μm thick), named 22-08-25 and ATLAS09 FBK12. Each sensor is bump-bonded to the corresponding number of FE-I4 readout chips, also developed for the IBL.

FE-I4 readout chips have 80 columns by 336 rows of $250\,\mu m \times 50\,\mu m$ pixel cells. Each cell amplifies the collected signal and compares it to a programmable threshold. While for the devices under test the minimal threshold is 1000 e^-, data were also collected at thresholds of 2000 e^- and 3000 e^-. In contrast, ITk modules are expected to have a minimal discriminator threshold of 600 e^-.

The time-over-threshold (ToT) is measured in units of the 25 ns clock signal. For each threshold value of interest, the devices under test were tuned to yield a ToT value of 10 units for a 16 ke^- signal. Noisy and malfunctioning pixels were masked during this process: the resulting noise rates as measured with a dedicated scan were <1 hit per minute in any given module.

In addition to testing the pixel modules at different incidence angles and threshold values, the sensors were tested in a range of reverse bias voltage values. Planar modules were operated fully depleted at 80 V or 120 V, while 3D modules require lower values: module 22-08-25 was operated most often at 9 V with a few runs at 2 V, and module ATLAS09 FBK12 was tested in a range from 2 V to 40 V. Except where discussed in Section 5, no difference in performance is observed for these bias voltage variations.