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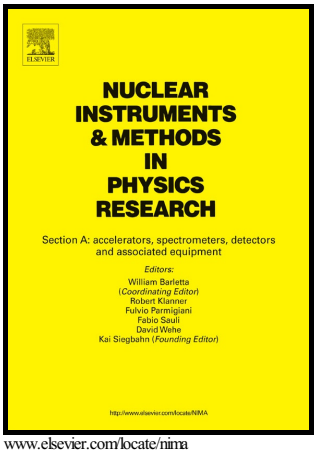

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Abstract

We report on the development of electronics hardware, FPGA firmware and software to provide a flexible multi-chip readout of the Timepix ASIC within the framework of the Scalable Readout System (SRS). The system features FPGA-based zero-suppression and the possibility to read out up to 4×8 chips with a single Front End Concentrator (FEC). By operating several FECs in parallel, in principle an arbitrary number of chips can be read out, exploiting the scaling features of SRS. Specifically, we tested the system with a setup consisting of 160 Timepix ASICs, operated as GridPix devices in a large TPC field cage in a 1 T magnetic field at a DESY test beam facility providing an electron beam of up to 6 GeV.

We discuss the design choices, the dedicated hardware components, the FPGA firmware as well as the performance of the system in the test beam.

Keywords: Timepix, SRS, Micro-pattern gaseous detectors, Pixel-TPC, ILC, GridPix

1. Introduction

The Timepix ASIC [1], derived from the Medipix-2 ASIC [2], has been widely used in combination with semiconductor pixel detectors as an X-ray imaging device [3–5]. In addition to this, its application as a pixelised active charge-sensing anode for gaseous detectors has been studied by several groups [6–8].

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