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Compensation for radiation damage of SOI pixel detector via tunneling

M. Yamada [a,*], Y. Arai [a], Y. Fujita [a], R. Hamasaki [b], Y. Ikegami [a], I. Kurachi [a], T. Miyoshi [a], R. Nishimura [b], K. Tauchi [a], T. Tsuboyama [a]

[a] High Energy Accelerator Research Organization (KEK), IPNS, Oho 1-1, Tsukuba, Ibaraki 305-0801, Japan
[b] SOKENDAI (The Graduate University for Advanced Studies), Shonan Village, Hayama, Kanagawa 240-0193, Japan

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ABSTRACT

We are developing a method for removing holes trapped in the oxide layer of a silicon-on-insulator (SOI) monolithic pixel detector after irradiation. Radiation that passes through the detector generates positive charge by trapped holes in the buried oxide layer (BOX) underneath the MOSFET. The positive potential caused by these trapped holes modifies the characteristics of the MOSFET of the signal readout circuit. In order to compensate for the effect of the positive potential, we tried to recombine the trapped holes with electrons via Fowler–Nordheim (FN) tunneling. By applying high voltage to the buried *p*-well (BPW) under the oxide layer with the MOSFET fixed at 0 V, electrons are injected into the BOX by FN tunneling. X-rays cause a negative shift in the threshold voltage V_{th} of the MOSFET. We can successfully recover V_{th} close to its pre-irradiation level after applying $V_{BPW} \geq 120$ V. However, the drain leakage current increased after applying V_{BPW}; we find that this can be suppressed by applying a negative voltage to the BPW.

1. Introduction

A hybrid type pixel detector is widely used for high-energy physics, X-ray imaging and so on. A sensor and a readout circuit are mechanically connected by a bump bonding [1,2]. However the bump bonding is not suitable for a fine spatial resolution, high speed readout and low power etc. Recently a monolithic type pixel detector has been developed to fulfill such requirements [3,4].

We are developing a monolithic pixel detector with silicon-on-insulator technology (SOIPIX) for charged particle trackers in high-energy physics, astrophysics, X-ray imaging, and so on [5–8].

A cross section of the SOIPIX is shown in Fig. 1. An LSI circuit for signal readout is fabricated on the SOI layer, which is above the buried oxide layer (BOX).

A buried *p*-well (BPW) is formed under the BOX to suppress the back-gate effect due to the bias voltage for the sensor. In most applications, the SOIPIX is required to have a high tolerance to radiation. The major cause of radiation damage is the trapped holes generated in the BOX. As radiation passes through the BOX, electron–hole pairs are generated. Since the hole mobility is lower than the electron mobility, the generated holes are trapped in the BOX [10]. The positive potential due to these trapped holes affects the MOSFETs and causes the readout circuit to malfunction. To compensate for such a total ionizing dose (TID) effect, we have studied a method for removing the holes trapped in the BOX via tunneling. Normally, radiation damage is annealed by heating the sensor at a high temperature. However, extracting the pixel detector from experimental equipment and annealing is not easy in most cases. The trapped holes can be removed by illumination with ultraviolet ultra-violet light, but it is difficult to illuminate the BOX region. Therefore, the damaged detector is replaced at the time of its lifetime in the experiments mentioned above.

We have been developing double-SOI technology. The additional silicon layer is used to suppress the back-gate effect and cross-talk and to compensate for the electric potential caused by the trapped holes [11,12]. However, it is not effective if the radiation damage is not uniform throughout the sensor. Additionally an appropriate voltage must be continuously supplied to the middle SOI layer. In order to cancel the positive potential, the voltage should be adjusted according to the accumulated dose, and we have to implement a circuit that automatically controls the voltage.

Fowler–Nordheim (FN) tunneling is utilized in this study and occurs at a high electric field around 0.5 GV/m [13]. It is possible to compensate for the positive charge in the BOX by the recombination of the trapped holes and the electrons injected via the FN tunneling. This method is suitable if the radiation damage is not uniform throughout the detector. The voltage for FN tunneling is determined by the electric field across the oxide layer.

* Corresponding author.
E-mail address: yamadami@post.kek.jp (M. Yamada).

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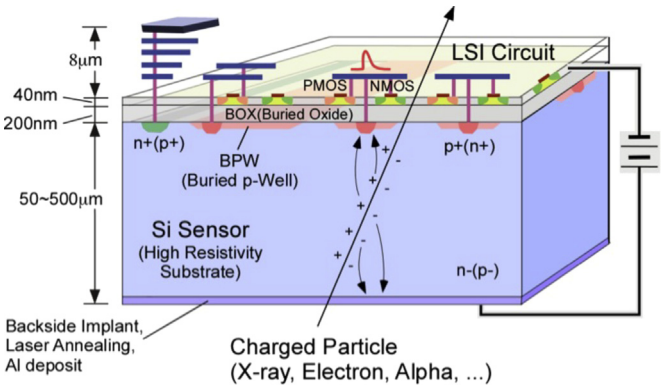

Fig. 1. Cross section of the SOI monolithic pixel detector. The readout circuit is processed on the top SOI layer. The buried oxide layer (BOX) is under the SOI layer. The buried *p*-well (BPW) is created under the BOX to suppress the back-gate effect. The voltage to the BPW can be supplied through the p^+ implant (PS). The thickness of silicon sensor under the BOX depends on application [9].

This means that the voltage only depends on the thickness of the BOX and not on the accumulated dose. In our previous study [14], we reported that the negatively shifted threshold voltage V_{th} of the MOSFET is recovered by applying 0.6 GV/m for 3 s.

2. Fowler–Nordheim tunneling

Electrons tunnel through the triangular potential of the Si–SiO_2 junction in Fig. 2. The FN tunneling current is expressed [15] as

$$J = AE_{ox}^2 \exp\left(-\frac{B}{E_{ox}}\right), \tag{1}$$

where A and B are written as follows:

$$A = \frac{e^3}{8\pi h \phi_B (m_{ox}^*/m_0)}, \tag{2}$$

$$B = \frac{8\pi\sqrt{2m_{ox}^*}\phi_B^{3/2}}{3he}, \tag{3}$$

where e is the electron charge, h is the Planck constant, ϕ_B is the barrier height of the Si–SiO_2 junction, m_{ox}^* is the effective mass of an electron, and m_0 is the rest mass of an electron. The FN tunneling current has a factor of the square of the electric field across the oxide layer E_{ox}. Therefore the FN tunneling current is very sensitive to the voltage supplied to the oxide layer compared with other tunneling mechanisms. If we rearrange Eq. (1) and take the logarithm of both sides, we obtain the following equation:

$$\ln\left(\frac{J}{E_{ox}^2}\right) = \ln(A) - \frac{B}{E_{ox}}. \tag{4}$$

From this equation, a plot of $\ln(J/E_{ox}^2)$ as a function of $1/E_{ox}$ should be linear, and this plot is called an FN plot. A high voltage pulse that exhibits linearity in the FN plot will be able to remove charges trapped in the BOX.

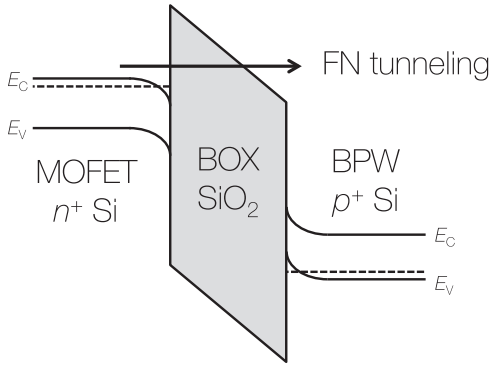

Fig. 2. Fowler–Nordheim tunneling. Electrons tunnel through the triangular potential of Si–SiO_2 junction. FN tunneling occurs at a high electric field of more than 0.5 GV/m.

3. Experimental procedure

A test element group of MOSFETs called TrTEG, which have different gate widths and lengths, was used to evaluate the characteristics of the MOSFETs before and after irradiation. The TrTEG was fabricated using a 0.2 μm FD-SOI CMOS process technology by LAPIS Semiconductor Co., Ltd. [16]. The thickness of the BOX was T_{BOX} = 200 nm. I_D–V_{GS} characteristics of the MOSFETs were measured with source measure units manufactured by Keithley Instruments, Inc. The TrTEG was irradiated with X-rays up to 50 kGy at KEK. The X-ray source is the X-ray tube of a copper target (Kα line of 8 keV). The source, drain, gate, and body of the MOSFETs and the BPW were connected to ground during irradiation to avoid charge-up of the sample. The I_D–V_{GS} characteristics at V_D = 1.8 V were measured before and after irradiation. V_{th} and the leakage current I_{leak} derived from the I_D–V_{GS} characteristics were used to evaluate the performance of the MOSFETs. V_{th} and I_{leak} are defined as

$$V_{th} = V_{GS} \quad \text{at } I_D = 0.1 \times W/L \ (\mu A), \tag{5}$$

$$I_{leak} = I_D \quad \text{at } V_{GS} = 0V. \tag{6}$$

To remove trapped charge from the BOX via FN tunneling, (1) a high voltage is applied between the MOSFET and the BPW, as shown in Fig. 3. The source, gate, and drain are fixed at 0 V. The body is fixed at 0 V in the case of a body-tie MOSFET. A high-voltage, from 10 to 150 V, is applied to the BPW (V_{BPW}) for a duration of 3 s. (2) After applying V_{BPW}, the I_D–V_{GS} characteristics with V_D = 1.8 V are measured, and V_{th} and I_{leak} are determined to evaluate the recovery of radiation damage. (3) Steps (1) and (2) are repeated while increasing V_{BPW} up to 150 V.

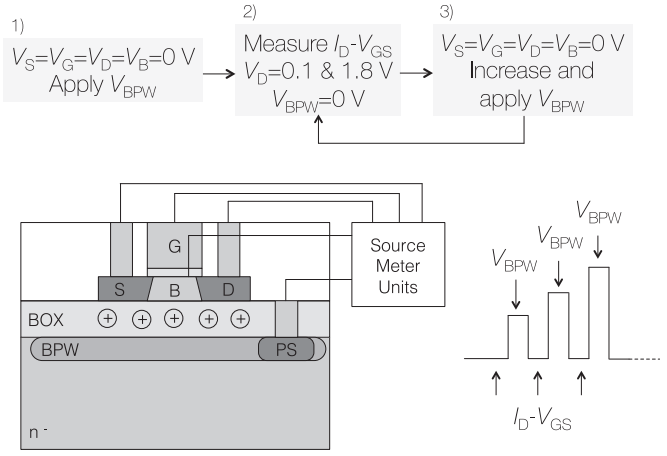

Fig. 3. Experimental setup and procedure for the measurement of the I_D–V_{GS} characteristics and V_{BPW} pulses. (1) High-voltage pulses of V_{BPW} are applied to the BPW with the source, gate, and drain fixed at 0 V for FN tunneling between the BPW and the MOSFET through the BOX. (2) Measurement of the I_D–V_{GS} characteristics with V_D = 1.8 V to evaluate V_{th} and I_{leak}. (3) Iteration of (1) and (2) up to V_{BPW} = 150 V.