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Prototypes and system test stands for the Phase 1 upgrade of the CMS pixel detector

S. Hasegawa, for the CMS Collaboration

Fermi National Accelerator Laboratory, PO Box 500, Batavia, IL 60510-5011, United States

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ABSTRACT

The CMS pixel phase-1 upgrade project replaces the current pixel detector with an upgraded system with faster readout electronics during the extended year-end technical stop of 2016/2017. New electronics prototypes for the system have been developed, and tests in a realistic environment for a comprehensive evaluation are needed. A full readout test stand with either the same hardware as used in the current CMS pixel detector or the latest prototypes of upgrade electronics has been built. The setup enables the observation and investigation of a jitter increase in the data line associated with trigger rate increases. This effect is due to the way in which the clock and trigger distribution is implemented in CMS. A new prototype of the electronics with a PLL based on a voltage controlled quartz crystal oscillator (QPLL), which works as jitter filter, in the clock distribution path was produced. With the test stand, it was confirmed that the jitter increase is not seen with the prototype, and also good performance was confirmed at the expected detector operation temperature (-20 °C).

1. Phase-1 upgrade project of the forward pixel detector

The CMS experiment [1] explores the fundamental laws governing elementary particles by studying proton–proton collisions at a center-of-mass energy of 13 TeV at the LHC [2] at CERN in Geneva, Switzerland. The innermost part of the CMS detector is a silicon pixel detector which allows for high precision tracking close to the interaction point. The pixel detector covers pseudorapidities up to 2.4 and detects charged particles emerging from beam collisions. It is divided into a barrel pixel detector and a forward pixel detector (FPIX). As the luminosity of the colliding beams is increased to $2\times10^{34}\,\mathrm{cm}^{-2}\,\mathrm{s}^{-1}$ in 2017, during the next few years, the readout chips on the present pixel modules would become inefficient, mainly due to buffer overflows. The pixel detector will be replaced by an upgraded detector with three disks of sensor modules with improved readout chips and faster readout electronics during the extended year-end technical stop of 2016/2017 in the "Pixel phase-1 upgrade" project [3].

Prototypes of new electronics have been developed and performance evaluation in an integrated system built with actual components is needed. In addition, the new FPIX detector, assembled at Fermi National Accelerator Laboratory (FNAL), needs to be fully tested and calibrated before it is shipped to CERN.

2. Test stand of full readout chain

The FPIX system is divided into front-end and back-end parts. The front-end consists of pixel sensor modules and readout electronics, and these are mounted in the CMS detector. The back-end system will be housed in a counting room next to the CMS detector cavern and controls the front-end electronics via optical fiber connections.

A test stand of the full readout system was set up at FNAL, using either the same hardware as used in the current CMS pixel detector or the latest prototypes of upgrade electronics. Fig. 1 shows the test stand at FNAL, which consists of several sensor modules (in the picture, one module is attached), electronics for their operation, and a VME back-end to control the modules.

The phase-1 upgrade detector system adopts the same scheme in many parts such as electronics control, and clock and trigger distributions, but one of the large differences is that the new sensor modules transmit digitized data at a rate of 400 Mbps while the current modules transmit analog encoded data at 40 MHz. In addition, the upgrade system will replace the VME back-end system by a μTCA system, which is under development. For the purpose of system development, a special add-on board was produced which is mounted on the current VME module for data readout, receives the 400 Mbps digitized data, and passes the data to the VME module in the same format as the current system.

The test stand adopts the same data acquisition system as the

E-mail address: satoshi@fnal.gov

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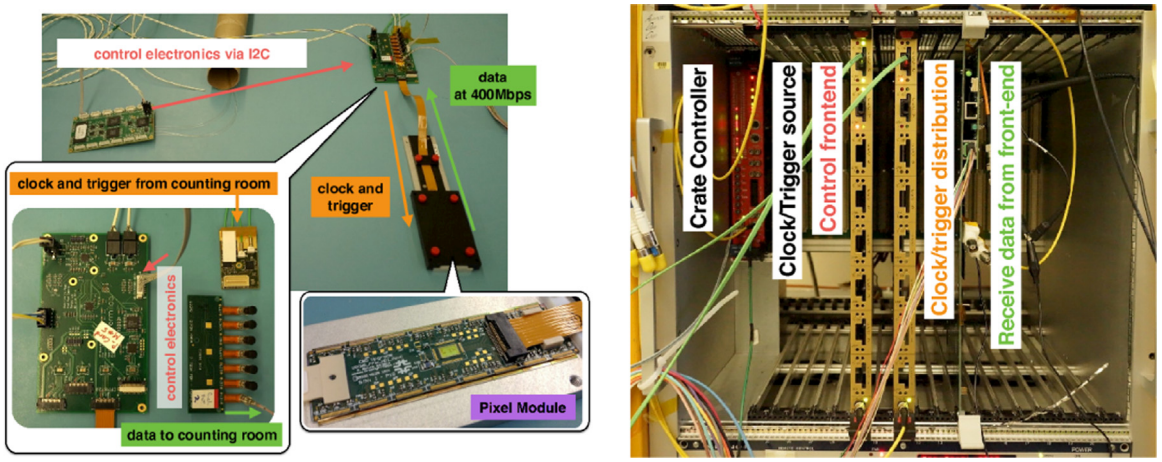

Fig. 1. Overview of the test stand set up at FNAL. The left part is the front-end side and consists of a sensor module, and control and readout electronics. The right part is the back-end side and the VME modules are for control of the front-end and readout.

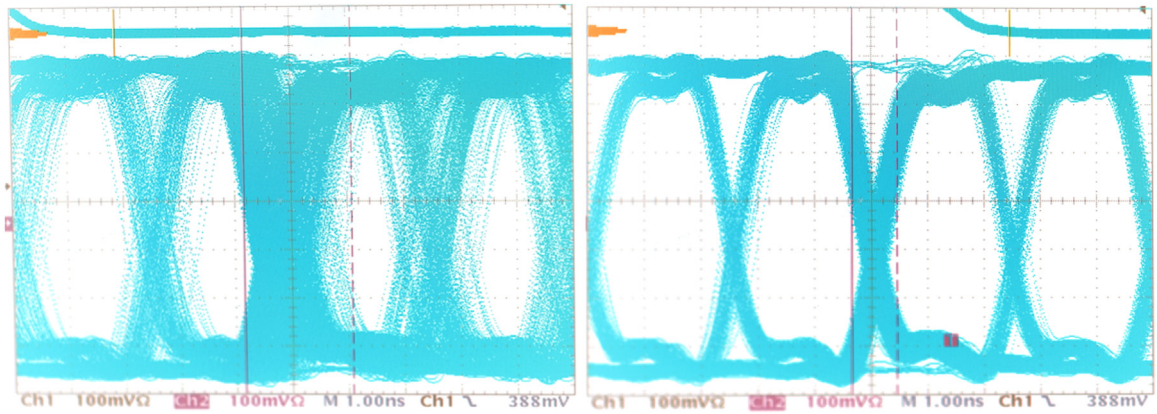

Fig. 2. Eye diagram of the data signal with a random trigger at a rate of 100 kHz with a previous prototype electronics in which only a TPLL is used in the clock path (left) and with a new prototype in which a QPLL and a TPLL are set in series (right). (The asymmetry of the waveform is due to a characteristic of the transmitter prototype on the detector module, and it has been solved in a new chip.).

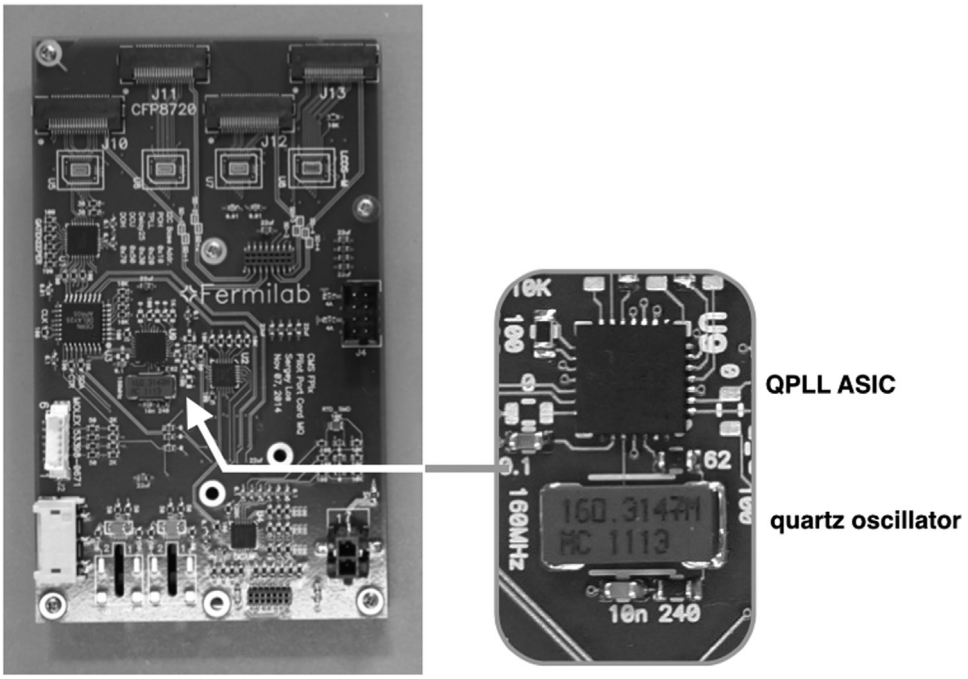

Fig. 3. New electronics prototype with the QPLL chip in the clock distribution system.

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