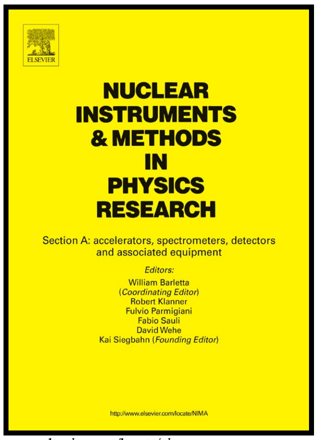

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Bo Kyung. Cha, Seongchae Jeon, Chang-Woo Seo

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X-ray performance of a wafer-scale CMOS flat panel imager for applications in medical imaging and nondestructive testing

Bo Kyung Cha[a], Seongchae Jeon[a], Chang-Woo Seo[b]

[a]*Advanced Medical Device Research Center, Korea Electrotechnology Research Institute, Ansan, Republic of Korea*

[b]*Department of Radiological Science, Yonsei University, Gangwon-do 220-710, Republic of Korea*

Abstract

This paper presents a wafer-scale complementary metal-oxide semiconductor (CMOS)-based X-ray flat panel detector for medical imaging and nondestructive testing applications. In this study, our proposed X-ray CMOS flat panel imager has been fabricated by using a 0.35µm 1-poly/4-metal CMOS process. The pixel size is 100µm x 100µm and the pixel array format is 1200x1200 pixels, which provide a field-of-view (FOV) of 120mm x 120mm. The 14.3-bit extended counting analog-to digital converter (ADC) with built-in binning mode was used to reduce the area and simultaneously improve the image resolution. The different screens such as thallium-doped CsI (CsI:Tl) and terbium gadolinium oxysulfide (Gd_2O_2S:Tb) scintillators were used as conversion materials for X-rays to visible light photons. The X-ray imaging performance such as X-ray sensitivity as a function of X-ray exposure dose, spatial resolution, image lag and X-ray images of various objects were measured under practical medical and industrial application conditions. This paper results demonstrate that our prototype CMOS-based X-ray flat panel imager has the significant potential for medical imaging and non-destructive testing (NDT) applications with high-resolution and high speed rate.

Keywords: X-ray scintillator; CMOS flat panel dector; Medical imaging ; NDT

1. Introduction

In recent years, CMOS (complementary metal oxide semiconductor) flat panel X-ray imagers have widely been developed and used in most medical and industrial imaging application for high resolution and real-time image. The CMOS flat panel imager has significant advantages such as cheaper cost than CCD and TFT technologies, higher readout speed due to electron mobility in crystalline silicon than in amorphous silicon, lower noise and high system integration. Specially, the CMOS flat panel X-ray imager has not only the higher readout rate (10 times faster speed) and lower readout noise because of lower transistor resistance in crystalline silicon but also, can include the readout and ADC (analog-digital converter) circuit on a silicon wafer substrate. In addition, the smaller pixel sized achieved in CMOS technology provides higher spatial resolution that is interesting for