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Capacitively coupled hybrid pixel assemblies for the CLIC vertex detector ☆

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ABSTRACT

The vertex detector at the proposed CLIC multi-TeV linear e^+e^- collider must have minimal material content and high spatial resolution, combined with accurate time-stamping to cope with the expected high rate of beam-induced backgrounds. One of the options being considered is the use of active sensors implemented in a commercial high-voltage CMOS process, capacitively coupled to hybrid pixel ASICs. A prototype of such an assembly, using two custom designed chips (CCPDv3 as active sensor glued to a CLICpix readout chip), has been characterised both in the lab and in beam tests at the CERN SPS using 120 GeV/c positively charged hadrons. Results of these characterisation studies are presented both for single and dual amplification stages in the active sensor, where efficiencies of greater than 99% have been achieved at −60 V substrate bias, with a single hit resolution of 6.1 μm. Pixel cross-coupling results are also presented, showing the sensitivity to placement precision and planarity of the glue layer.

1. Introduction

The demands for precision physics in combination with the challenging experimental conditions at the proposed electron-positron Compact LInear Collider (CLIC) have inspired a broad detector R&D program [1]. In particular the vertex-detector systems have to fulfil unprecedented requirements in terms of material budget (0.2% of a radiation length, X_0, per layer) and spatial resolution (3 μm single-point resolution) in a location close to the interaction point, where the rates of beam-induced background particles are high. Time slicing of hits with an accuracy of approximately 10 ns will be required to separate such backgrounds from physics events.

The R&D aims at achieving the single-point resolution target with a pixel size of $25 \times 25\ \mu m^2$ and analogue readout. Hybrid readout solutions are currently under study, comprised of high-performance readout Application Specific Integrated Circuits (ASICs) coupled to ultra-thin sensors with fast signal collection through drift in the depleted bulk volume. The target thickness for ASICs and sensors is 50 μm each.

Conventional small-pitch solder bump bonding between the readout ASICs and the sensors is costly and reduces the achievable yield for large-area detector systems. Moreover, planar high-resistivity passive sensors require the use of complex and costly custom manufacturing processes. The use of Capacitively Coupled Pixel Detectors (CCPD) has recently been proposed as an alternative [2]. In this approach active sensors with an amplification stage in each pixel are implemented in a commercial High-Voltage Complementary Metal-Oxide-Semiconductor process (HV-CMOS). The sensor substrate is biased, leading to a depletion layer of a few microns. The fast drift signal collected in this depleted layer is transformed to a voltage signal by a transimpedance amplifier and sent to a metal readout pad. This voltage signal is then capacitively coupled through a thin (few microns) layer of glue to the corresponding input pixel pad of the readout ASIC.

In the following chapters we present first laboratory and test-beam measurement results for prototypes of an active HV-CMOS sensor (CCPDv3) capacitively coupled to a readout ASIC (CLICpix).

2. Capacitively coupled pixel detectors

2.1. The CCPDv3 HV-CMOS sensor

The CCPDv3 is an ASIC implemented in a 180 nm high-voltage CMOS process, designed specifically for use as an active sensor.

☆This work was carried out in the framework of the CLICdp collaboration.

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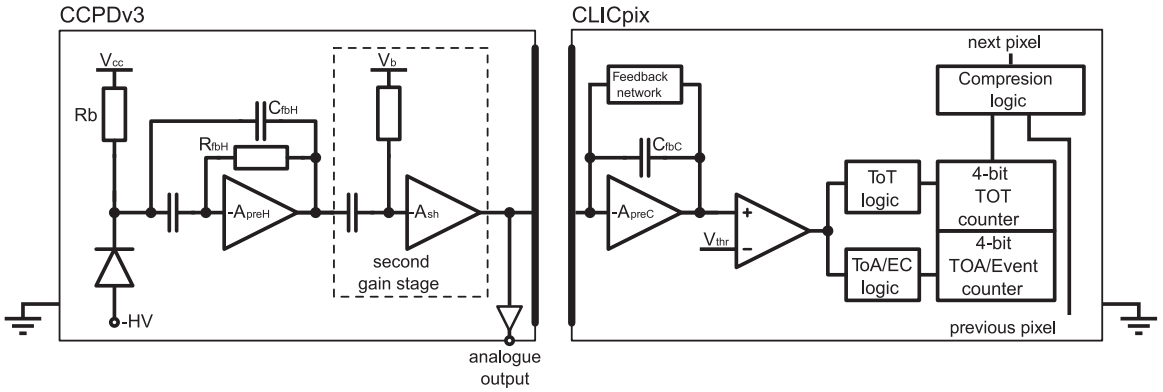

Fig. 1. Schematic of the CCPDv3 and CLICpix pixels, with two-stage amplification shown on the CCPDv3.

The chip contains 64 × 64 pixels with no standalone readout circuitry, except for a single line through which the analogue output of individual pixels may be probed. Each 25 × 25 μm^2 pixel contains only analogue circuitry, placed in a deep n-well which acts as the collection electrode (on the p-type substrate) in addition to providing shielding for the electronics and allowing the application of a substrate bias of up to −60 V. This allows the creation of a depletion region around the deep n-well, providing fast carrier collection and increased signal size compared to that available solely through diffusion. Nonetheless, due to the low resistivity of the substrate (10 – 20 Ω cm) the active depth is not expected to exceed 30 μm. The deposited charge is amplified by an integrating amplifier, with an optional second stage voltage amplifier, and the resulting voltage is directed towards an output pad. This pad is then connected to the readout chip by capacitive coupling.

Simplified schematics of the pixel designs for the CCPDv3 and CLICpix (described below) are shown in Fig. 1. The CCPDv3 pixel contains two amplification stages, and is the default design implemented through most of the chip. A four-column region however contains pixels with a slightly modified architecture, where the second stage is removed. The resulting voltage pulse is of opposite polarity, and is reduced in magnitude by a factor of approximately 2. This reduction in amplification should result in lower power consumption, which is of considerable interest for CLIC.

The leakage current of the chip versus applied bias voltage is shown in Fig. 2, where the current is observed to be satisfactory (at the level of tens of nA) until −93 V, well in excess of the maximum rating (– 60 V). This is the maximum operation voltage guaranteed by the manufacturer to have no negative effect on the device performance, though for the tests below a substrate voltage of up to −80 V was applied in order to maximise the charge collected.

2.2. The CLICpix readout ASIC

The CLICpix demonstrator hybrid readout chip [3] is a small prototype ASIC targeted to the requirements of the CLIC vertex detector. The chip is implemented in a 65 nm CMOS process. It contains a matrix of 64 × 64 pixels with 25 μm pitch, containing both analogue and digital functionality. Each pixel contains two 4-bit counters, with configurable modes, which operate simultaneously. A Time over Threshold (ToT) measurement of the injected charge amplitude has been implemented, incrementing the counter for each clock cycle during which the discriminator output remains high. A counting mode has also been implemented, incrementing the counter each time the discriminator exceeds the set threshold. Finally, time-stamping of the event is possible by measuring the time between the discriminator crossing threshold and the shutter (described below), to give the particle Time of Arrival (ToA).

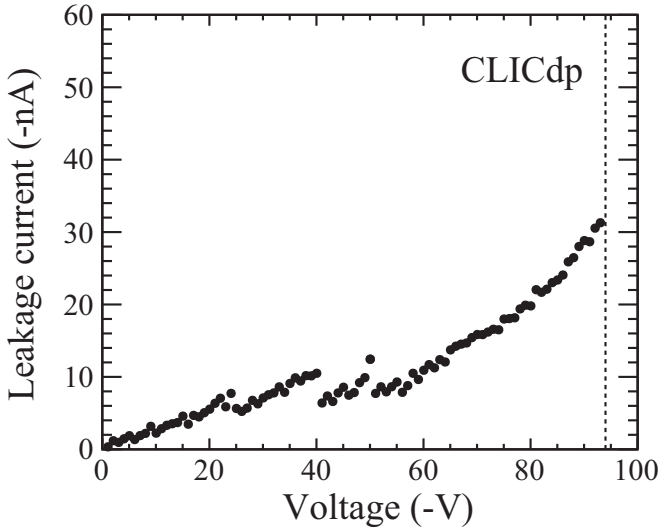

Fig. 2. High voltage tolerance of the CCPDv3, showing the leakage current versus bias voltage for the full 1.6 × 1.6 mm^2 matrix. The breakdown voltage is indicated by the dashed line.

The readout architecture of the CLICpix is designed to match the expected beam structure at the CLIC accelerator, involving bunch-train periods of 156 ns with intense activity followed by gaps of 20 ms used for the readout. This is most suited to a shutter-based operation of the chip, whereby all pixels are continuously sensitive while the shutter is open, after which the full matrix is read out. Zero compression is performed on the ASIC level, and the full chip can be read out in less than 800 μs (for 10% occupancy), using a 320 MHz readout clock. A custom readout system, built on a SPARTAN6 FPGA board and modular interface card [4], has been designed for this purpose. Initial testing (without sensor) has shown that the CLICpix is fully functional and that the performance is in agreement with simulations [5]. For all of the results shown, the ToT measurement of the input charge was performed using a clock frequency of 20 MHz and a constant discharge current.

2.3. Capacitively coupled assemblies

First assemblies of capacitively (or AC) coupled CLICpix ASICs with CCPDv3 active sensors were produced and tested in October 2014. Two mechanical samples were produced for cross-section measurements, while the results shown below are from a single assembly produced to validate the concept of capacitively coupled